ECE 3274 BJT amplifier design CE, CE with Ref, and CC.

Richard Cooper

Section 1: CE amp Re completely bypassed (open Loop)

Section 2: CE amp Re partially bypassed (gain controlled).

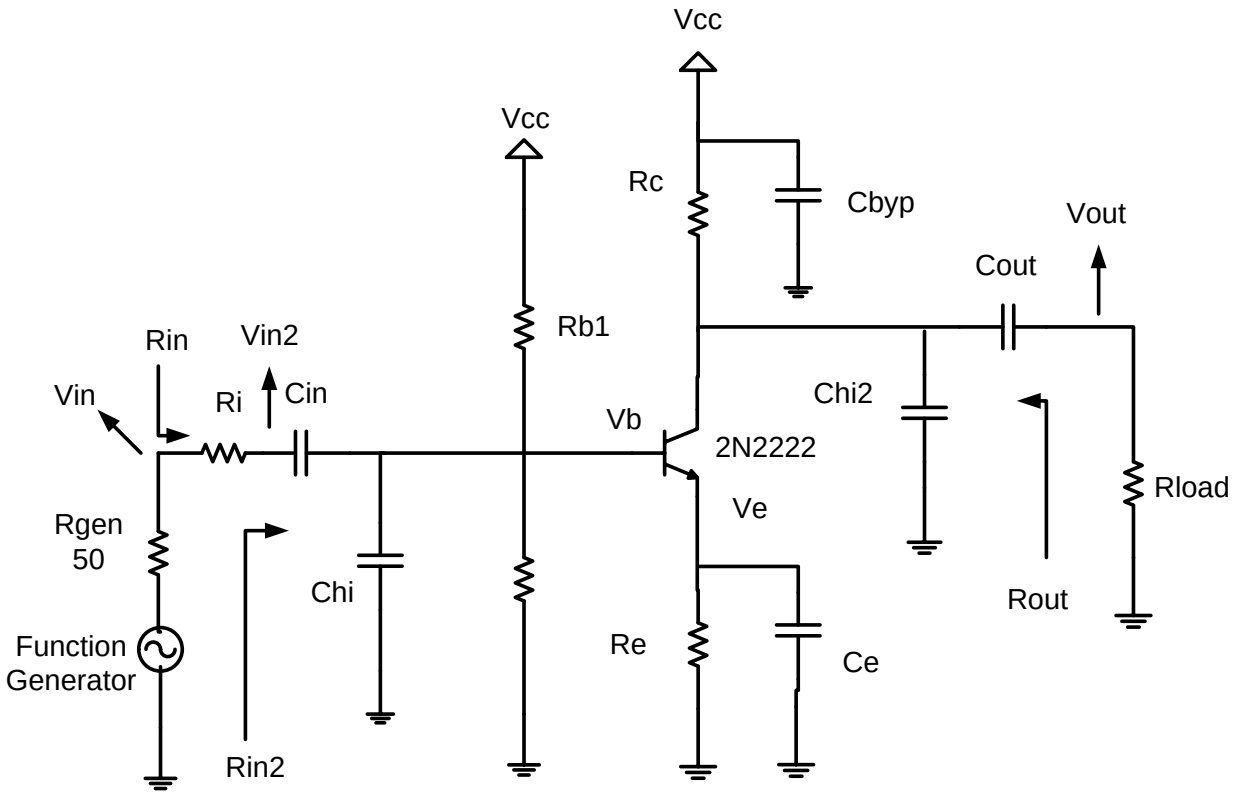
Section 3: CC amp (open loop)

Section 1: Common Emitter CE Amplifier Design

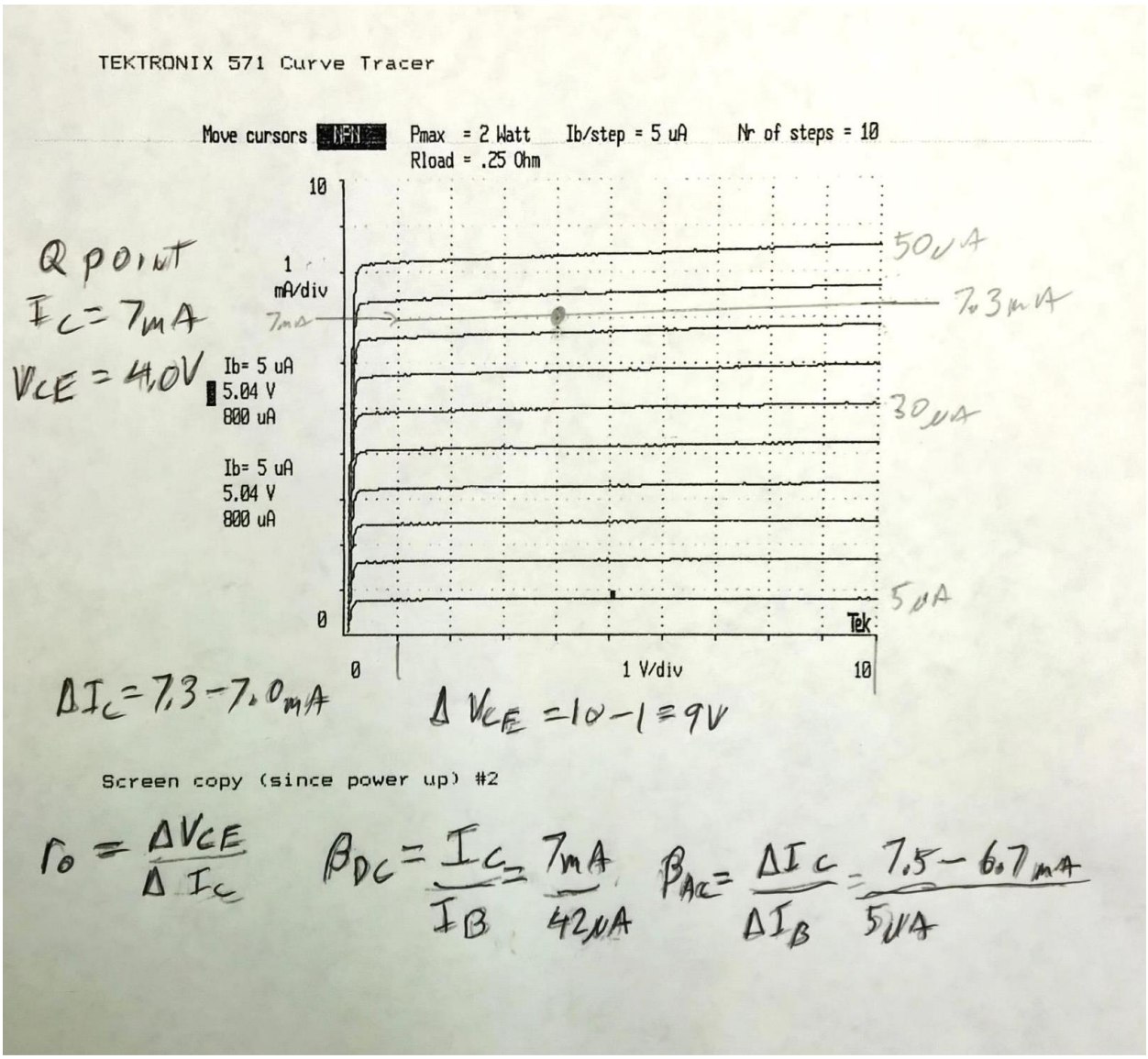
Vout is inverted so the gain Av and Ai are negative.

Designing procedure of common emitter BJT amplifier has three areas. First, we have to set the Q-point, which is the DC operating point. Since, no specification regarding the Q-point is mentioned in the design requirements; it leaves the designer enough freedom to choose the operating point as necessary for the application. However, remember that the specifications given in terms of input and output impedance, gain, frequency response characteristics and peak output voltages ultimately restricts the Q-point in a narrow window. It is difficult derive the Q-point without some intelligent guess and the following steps would work out for the given conditions. We will start to choose a Q-point to allow maximum output voltage swing.

In this configuration, R_E is completely bypassed. The circuit diagram with necessary variables is provided in CE Figure 1.



CE Figure 1: BJT Common Emitter



BJT Figure 2: BJT characteristics. The example not your Q-point

Step CE 1.1: Measure the device parameters

For the design of the amplifier, the 3 parameter values required are r_o and gm. Derived from the transistor characteristics curve shown in CE Figure 2, one can set an approximate Q-point (V_{CE} and I_C) in the active region and measure ro and β. We will solve for V_{ce} and estimate I_C.

Solve for V_{CE} see below **Step CE2.2** . Use Vout peak to find I_{load} peak: Iload = Vout / Rload.

For an approximate I_C Q-point use $I_C \approx 2.2 * I_{load}$ peak this is not the solution to your design Q-point. We can use an approximate I_C because ro and β will not very much with small changes in Q-point.

The Vce_{SAT} (Vce saturation voltage) is found from the BJT characteristics curve where the curve begins to flatten out ≈ 0.2 Vdc.

$ro = \Delta V_{CE} / \Delta I_C$ the slope of a line thru Q-point

$\beta_{AC} = \Delta I_C / \Delta I_B$ measured around Q-point

Vce_{SAT} = Vce begins to flatten

$r_\pi = (\beta V_T) / I_C$ r_π is base to emitter resistance Hybrid Pie model.

Where $V_T = kT/q$ at room temperature is $V_T \approx 26mV$.

Plot the estimated Q-point (V_{CE},I_C) on the BJT characteristics curve.

Plot the estimated Q-point (V_{CE},I_C) on the BJT characteristics curve.

CE Part 2: Determine the Q-point.

Start with your BJT and selecting 4 resistors.

Step CE2.1: Choose V_E

Because V_{BE} will decrease ≈ 2.5mV / ˚ C rise we set V_E = between 2V to 3V. V_E and R_E will provide negative feedback to stabilize β and V_{BE}.

Step CE2.2: Calculate the midpoint V_C with Re complete bypassed Re = Reb, and Ref = 0

Midpoint selection will allow for maximum output voltage swing.
We will add 20% to Vout so the design is not on the edge of the solution.

$V_{C(max)} = V_{CC}$ - (Vout + 20%Vout)
$V_{C(min)} = V_E + V_{CE}$ sat + (Vout + 20%Vout)
$V_C = (V_{C(max)} + V_{C(min)}) / 2$ Midpoint V_C Q-point
$V_{CE} = V_C – V_E$ This is the Q-point V_{CE}

Step CE2.3: Calculate R_C .
The DC equation: $V_{CC} – V_C = V_{RC} = R_C I_C$ voltage across Rc derived from Vcc and Q-point Vc.
The AC equation: $Vout = i_c (R_C || r_o || R_L)$ output voltage $Vout_{peak}$
Rewrite: $Vout = i_c Rc (r_o || R_L) / (Rc + (r_o || R_L))$ Parallel resistance equation
Substituting in $v_{RC} = i_c R_C$
Combined equation: $Vout = V_{RC} (r_o || R_L) / (Rc + (r_o || R_L))$

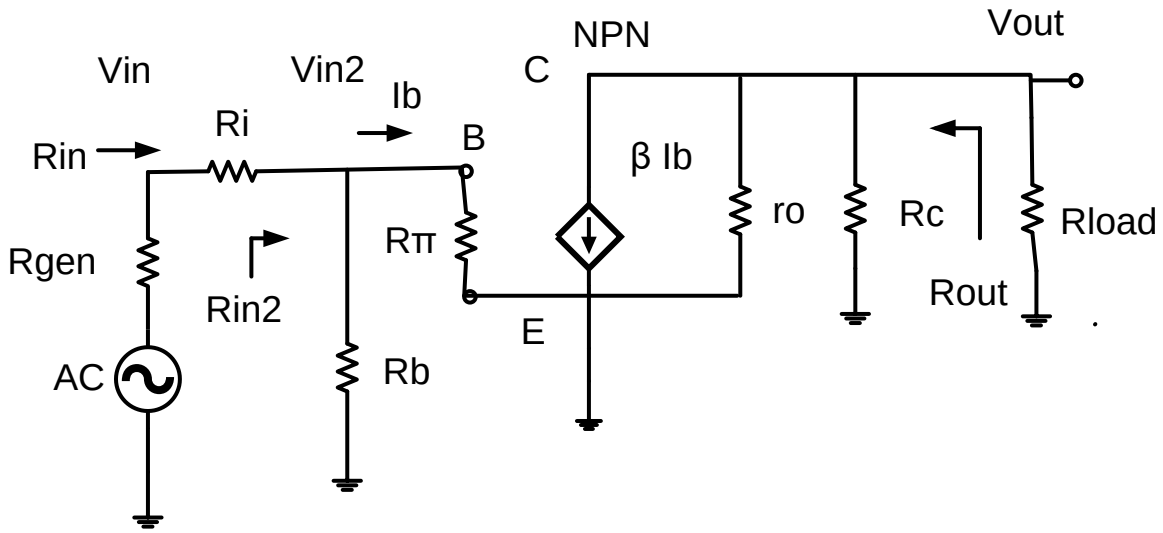
Solve for Rc; Add 20%Vout so the collector current is not set to an edge.

$$R_C = \frac{V_{CC} - V_C}{V_{out} + 20\% Vout} (r_o \parallel R_L) - (r_o \parallel R_L)$$

Step CE2.4: Calculate I_C, I_E, and Re.

$I_C = (V_{CC} - V_C) / R_C$ The Q-point collector current.
$I_B = I_C / \beta$ The base current.

$I_E = I_C (\beta + 1) / \beta$ emitter current.
$Re = V_E / I_E$ Total emitter resistance.
Thus, Q-point is (V_{CE}, I_C).



CE Figure 3: Common Emitter Small Signal Equivalent Circuit

CE Part 3: Determine bias resistors.

Step CE3.1: Calculate R_E. Design for the sum Ref and Reb
Later we will design for a desired Av (voltage gain) by using (Ref) and (Reb) to control the Av.
R_E = Ref + Reb
$I_E = I_C (\beta + 1) / \beta$
$I_B = I_C / \beta$
$\therefore R_E = \frac{V_E}{I_E}$

Step CE3.2: Calculate R_{b1}, R_{b2}. Method 1.
(Do not use Method 1 for your design.) Use step CE 3.3

$V_B = V_E + V_{BE}$ V_{BE} is normally between 0.6V and 0.7V

$Ib = Ic / \beta$

Current thru Rb1 is set to 10 * I_B
Current thru Rb2 is set to 9 * I_B
$Rb1 = (Vcc – V_B)/ (10* I_B)$
$Rb2 = V_B / (9 * I_B)$

Step CE3.3: Calculate R_{b1}, R_{b2}. Method 2.
(Use this Method)

Require Rin set to a given value. Need Vcc, Vb, r_π and Ib.
Given Rin calculate Rin2.

Rin2 = Rin –Ri Solve Rin2 needed to Rin requirements.

Solve for Rb from Rin2 and Rbase.
Rbase = r_π Re completely bypassed.
Rb = 1 /((1 / Rin2) – (1 / Rbase)) Solve for Rb needed to Rin requirements.

Find Rb1 first then Rb2
Rb1 = Vcc / ((Vb / Rb) + Ib) Solve for Rb1.
Rb2 = Vb / (((Vcc –Vb) /Rb1) –Ib) Solve Rb2 from Vb and current thru Rb2: $Irb2 = Ir_{b1} – Ib$

Check Rin meets requirements
Rbase = r_π Re completely bypassed.

Rb = Rb1 || Rb2.

Rin2 = Rb || Rbase

Rin = Ri + Rin2

CE Part 4: Calculating impedance and Gain

Vout is inverted so the Voltage gain Av is negative.

Refer to the small signal equivalent of the circuit you have just built in CE Fig. 3. We can calculate the following:

Step CE4.1: Input Impedance: AC characteristics

Rb = Rb1 || Rb2 the two base bias resistors.

If Re completely bypassed with C_E then

Rbase = r_π

Rin2 = Rb || Rbase

Rin = Ri + Rin2

Step CE4.2: Output Impedance

If Re **completely** bypassed with C_E then

Rout = R_C || r_0. With Ref = 0

Step CE4.3: Voltage Gain
AC voltage Vout = - β Ib (Rout || Rload || ro) Note: use the correct Rout depending on Ref
AC voltage Vin = (Rin/Rin2) Vin2 Input signal from the function generator.
AC voltage Vin2 = v_b Input signal on the base

Av2 = Vout / Vin2 = -β (Rc || ro || Rload) / r_π voltage gain at base. Av2 is negative.

Av = Vout / Vin = - β (Rc || ro || Rload) / ((Rin2+Ri) / Rin2) (r_π) Av is negative.

Rearrange Av = - β (Rin2 / (Rin2 + Ri)) * (Rd || ro || Rload) / r_π

Vgen = ((Rin + Rgen) / Rin) * (Vout/ Av) the open circuit voltage of the function generator.

Step CE4.4: Current Gain

$$\mathrm{Ai} = \frac{Iload}{Iin} = \frac{Vout/_{Rload}}{Vin/_{Rin}} = \mathrm{Av}\frac{\mathrm{Rin}}{\mathrm{Rload}}$$

Step CE4.5: Power gain
G = Pout / Pin = Vout * Iload / Vin * Iin = Av * Ai
In decibels G_{dB} = 10log (Av * Ai)

Step CE4.6: Vin and Voc of Vgen
Input signal level need to produce the required output voltage.
Vin = Vout / Av

The open circuit voltage of the generator to produce the required output voltage.
Because of Voltage divider because the output impedance of the Rgen = 50Ω

Vgen = Vin (Rgen + Rin) / Rin

Use this value in LTspice and the laboratory Function generator

CE Part 5: Frequency response

With the Q-point being set after the sequence of steps, we can go for the selection of capacitors and finally connect the signal generator at input and measure the output amplified waveform.

First we will select C_{in}, C_{out} and C_E which jointly would set the roll-off beyond the lower cut-off frequency. Set any frequency within the range as your lower cut-off frequency and let us call it f_L. Three capacitors will introduce 3 zeros in the transfer function of the system. Because we will set 3 zeros at the same frequency we must use the Band Width Shrinkage factor.

$$\text{BWshrinkage} = \sqrt{2^{\frac{1}{n}} - 1}$$

Where n is the number of zeros for low frequency breakpoints at same frequency.

$$f_L = \frac{f_{C_{in}} + f_{C_{out}} + f_{C_E}}{3\sqrt{2^{\frac{1}{3}} - 1}}$$

Setting 3 frequencies equal, we get,

$f_{Cin} = f_{Cout} = f_{CE} = f_L \sqrt{2^{1/3} - 1}$

Find the C for each breakpoint f_{Cin} , f_{Cout} , and f_{CE} where n = 3.

$$C = \frac{1}{2\pi f_C \,(\text{R seen by C})}$$

Where C is the capacitor that sets the breakpoint f_C

RemitterBase is the impedance looking in the BJT emitter to base.

RemitterbBase = (r_π + Rb || (Ri + Rgen)) / (β + 1) Small value

R is the Thevenin equivalent resistance seen by the capacitor.

R_{CE} = Re || (ro + R_C || R_{Load}) || RemitterBase)

The following table enlists the particular expressions.

Rsig	Rgen+Ri
C_{in}	Rsig + Rin2
Cout	RLoad + Rout
C_E	Re || ((ro + R_C || R_{Load}) || RemitterBase)
C_{hi}	Rsig || Rin2
C_{hi2}	Rout || Rload

CE Table 1: Resistance Seen By Capacitors

In this case because Chi, and Ch2 are to the same break point. We must use the band shrinkage factor with n = 2. We need only to find a two poles at F_h / bandshrinage = $f_{chi} = f_{ch2}$ to set the high frequency cutoff.

Set Fchi = Fchi2 = Fh / $\sqrt{2^{1/2} - 1}$

Rb = Rb1 || Rb2

Rbase = r_π

Rin2 = Rb || Rbase

R seen by C_{hi} R_{Chi} = (Rgen + Ri) || Rin2

$$C_{hi} = \frac{1}{2\pi f_{Chi}\,(\text{R seen by } C_{hi})}$$

R seen by C_{hi2} R_{Chi2} = Rout || Rload Note: use the correct Rout depending on Ref

$$C_{hi2} = \frac{1}{2\pi f_{Chi2}\,(\text{R seen by } C_{hi2})}$$

Section 2:

CEwRef Common Emitter with Re that partially is bypassed by Ce.

Vout is inverted so the gain Av and Ai are negative.

R_E = Ref + Reb the total R_E for the DC bias design.

Ref is the portion of Re that is not bypassed by Ce.

Reb is the portion of Re that is bypassed by Ce.

CEwRef Part 1: Measure the device parameters

For the design of the amplifier, the 3 parameter values required are Vce_{SAT}, r_o and β. Derived from the transistor characteristics curve shown in BJT Figure 2 above, one can set an approximate Q-point (V_{CE} and I_C) in the active region and measure ro and β. We will solve for V_{ce} and estimate I_C.

Solve for V_{CE} see below **Step CEwRef 2.2**. Use Vout peak to find I_{load} peak: Iload = Vout / Rload.

For an approximate I_C Q-point use $I_C \approx 2.2 * I_{load}$ peak this is not the solution to your design Q-point. We can use an approximate I_C because ro and β will not very much with small changes in Q-point.

The Vce_{SAT} (Vce saturation voltage) is found from the BJT characteristics curve where the curve begins to flatten out ≈ 0.2 Vdc.

ro = $\Delta V_{CE} / \Delta I_C$ the slope of a line thru Q-point

$\beta_{AC} = \Delta I_C / \Delta I_B$ measured around Q-point

Vce_{SAT} = Vce begins to flatten

$r_\pi = (\beta V_T) / I_C$ r_π is base to emitter resistance Hybrid Pie model.

Where $V_T = kT/q$ at room temperature is $V_T \approx 26mV$.

Plot the estimated Q-point (V_{CE},I_C) on the BJT characteristics curve.

CEwRef Part 2: Determine the Q-point.

Start with your BJT and selecting 4 resistors.

Step CEwRef 2.1: Choose V_E

Because V_{BE} will decrease ≈ 2.5mV / ˚ C rise we set V_E = between 2V to 3V. V_E and R_E will provide negative feedback to stabilize β and V_{BE}.

Step CEwRef 2.2: Calculate the midpoint V_C with Re partially bypassed Re = Reb + Ref

Midpoint selection will allow for maximum output voltage swing.

We will add 20% to Vout so the design is not on the edge of the solution. This will also help with the additional loading because of high frequency capacitors as the frequency approaches the high frequency break points.

$V_{C(max)} = V_{CC}$ - (Vout + 20%Vout)

$V_{C(min)} = V_E + V_{CE}$ sat + (Vout + 20%Vout)

$V_C = (V_{C(max)} + V_{C(min)}) / 2$ Midpoint V_C Q-point

$V_{CE} = V_C - V_E$ This is the Q-point V_{CE}

Step CEwRef 2.3: Calculate R_C .

Looking into the collector we see r_o + Ref || [(r_π + Rb1|| Rb2 || (Ri +Rgen)] / (β +1) ≈ r_o so we will use just r_o .

The DC equation: $V_{CC} - V_C = V_{RC} = R_C I_C$ voltage across Rc derived from Vcc and Q-point Vc.

The AC equation: Vout = i_c (R_C || r_o || R_L) output voltage $Vout_{peak}$

Rewrite AC: Vout = i_c Rc (r_o || R_L) / (Rc + (r_o || R_L)) Parallel resistance equation

Substituting in $v_{RC} = i_c R_C$

Combined equation: Vout = V_{RC} (r_o || R_L) / (Rc + (r_o || R_L))

Solve for Rc; Add 20%Vout so the collector current is not set to an edge.

$$R_C = \frac{V_{CC} - V_C}{V_{out} + 20\% Vout} (r_o \parallel R_L) - (r_o \parallel R_L)$$

Step CEwRef 2.4: Calculate I_C, I_E, and Re.

$I_C = (V_{CC} - V_C) / R_C$ The Q-point collector current.

$I_B = I_C / \beta$ The base current.

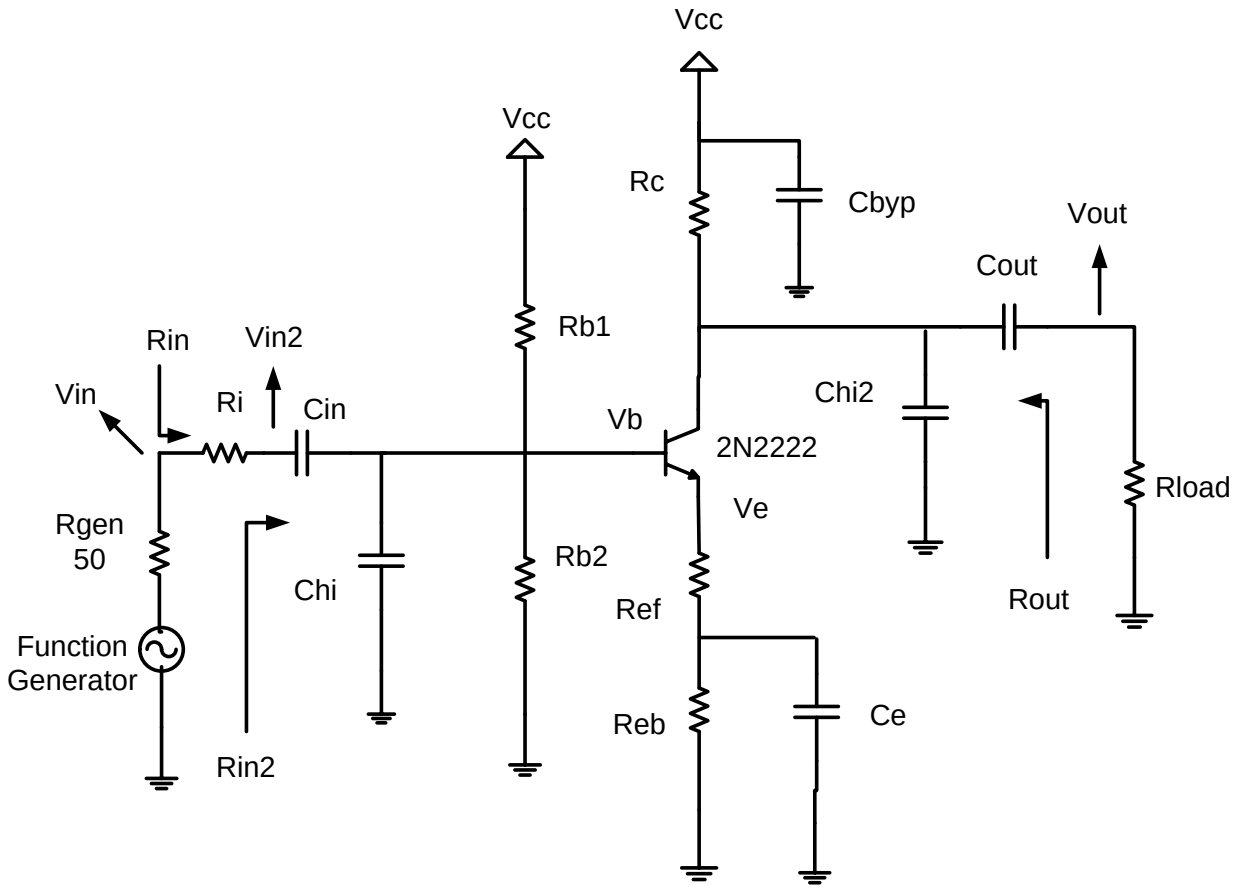
$I_E = I_C (\beta + 1) / \beta$ emitter current.

$Re = V_E / I_E$ Total emitter resistance.

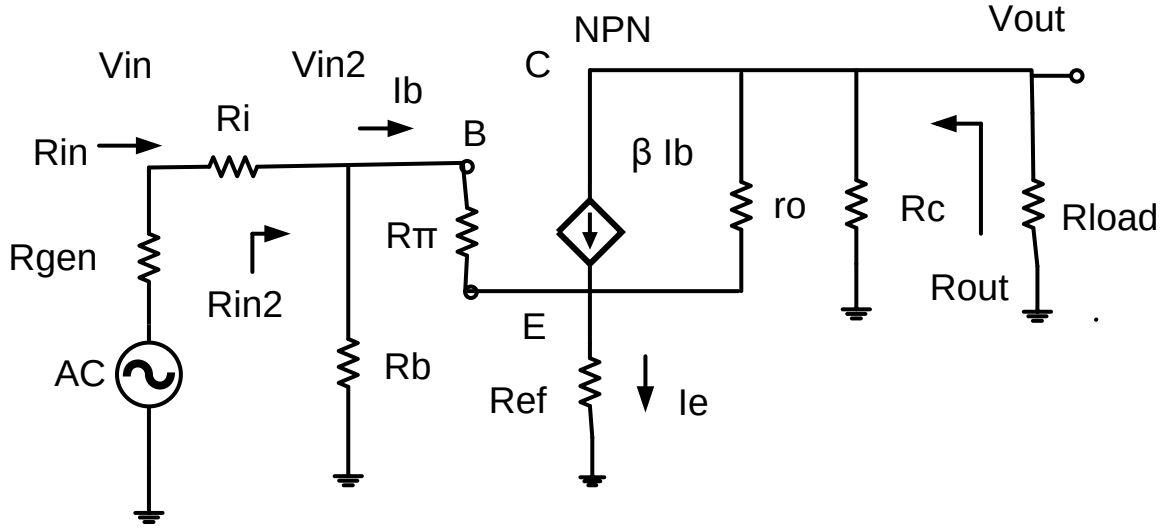
Thus, Q-point is (V_{CE}, I_C).

We have already choose V_E to be between 2V to 3V to provide negative feedback in the DC bias circuit. We will use Ve and I_C where Ie = ((β +1) / β) Ic. Now calculate Re =Ie (Ref +Reb) the total emitter resistance.

We now have, Ve, Vc, Rc, Re, Ic, Ie, Vce, Vce_{SAT}



CEwRef Figure 1: Amplifier with emitter partially bypassed.



CEwRef Figure 2: Small signal model with partial bypass of Re

CEwRef Part 3 Calculating impedance and Gain with Ref

Remember the gain Av and Ai are negative for a common emitter amplifier.

We use the same Q-point and bias resistors Rb1, Rb2, Rc, and Re = Ref + Reb.

Step CEwRef3.1: find Ref based on Voltage Gain requested
Note: i_b is the AC base current that results from Vin.
Looking into the collector we see ro + Ref || [(rπ + Rb1|| Rb2 || (Ri +Rgen)] / (β +1) ≈ ro so we will use just ro .
AC voltage Vout = - β i_b (Rc || Rload || ro) Note: use the approximant ro because Ref is not known yet.
AC voltage Vin = (Rin/Rin2) Vin2 Input signal from the function generator.
AC voltage Vin2 = i_b(rπ + (β + 1) Ref) Input signal on the base

Given Rin calculate Rin2.

Rin2 = Rin –Ri Solve Rin2 needed to meet the Rin requirements.

Av2 = Av * Rin / Rin2 Av2 at base needed to meet Av requested. For CE Av is negative.

Av2 = Vout / Vin2 = -β (Rc || ro || Rload) / (r_π + (β + 1) Ref) voltage gain at base, we do not need to find i_b since i_b cancels. Av2 is negative which means that Vout is inverted.

Step CEwRef3.2: Solve for Ref by using **gain at base Av2**.

Ref = = [(-β (Rc || ro || Rload) / Av2) - r_π] / (β + 1) from Av2 or use equation below

Step CEwRef3.3: Solve for Ref by using **overall gain Av**.

Av = Av2 * Rin2 / Rin

Av = Vout / Vin = - β (Rc || ro || Rload) / (Rin/Rin2) (r_π + (β + 1) Ref) voltage gain at input

We can see that voltage gain **Av** can be controlled by the value of **Ref**

Av = - β (Rin2/Rin) (Rc || ro || Rload) / (r_π + (β + 1) Ref)

Rearrange Av to solve for Ref from requested Av

Ref = -((β (Rin2/Rin) (Rc|| ro || Rload) / Av) - r_π) / (β + 1) from Av overall gain, Av is negative

Step CEwRef3.4: Solve for Reb from Re and Ref

Remember that Re is the total emitter residence from step CEwRef 2.4.

Reb = Re – Ref

Step CEwRef4.1: Rb1 and Rb2 based on requested Rin

Require Rin set to a given value. Need Vcc, Vb, r_π and I_B (DC bias base current).
Given Rin calculate Rin2.

Rin2 = Rin –Ri Solve Rin2 needed to meet the Rin requirements.

Solve for Rb from Rin2 and Rbase.

Rbase = r_π + (β + 1) (Ref || (ro + Rc || Rload)) Looking into the Base of the BJT.

Rb = 1 /((1 / Rin2) – (1 / Rbase)) Solve for Rb needed to Rin requirements.

Find Rb1 first then Rb2
$I_B = I_C / \beta$ DC bias base current.
Rb1 = Vcc / ((Vb / Rb) + Ib) Solve for Rb1.
Rb2 = Vb / (((Vcc –Vb) /Rb1) –Ib) Solve Rb2 from Vb and current thru Rb2: $Irb2 = Ir_{b1} – Ib$

Check Rin meets requirements
Rbase = r_π + (β + 1) (Ref || (ro + Rc || Rload)

Rb = Rb1 || Rb2.

Rin2 = Rb || Rbase

Rin = Ri + Rin2

Step CEwRef4.2: Input Impedance: AC characteristics

Rb = Rb1 || Rb2

Where Ref is the part of R_E that is not bypassed by C_E.

Rbase = r_π + (β + 1) (Ref || (ro + Rc || Rload)) Looking into the Base of the BJT.

Rin2 = Rb || Rbase

Rin = Ri + Rin2

Step CEwRef4.3: Output Impedance with Ref

If Re partially bypassed with C_E bypassing Ref.

Rb = Rb1 || Rb2.

RemitterBase is the impedance looking in the BJT emitter toward the base.

RemitterBase = (r_π + Rb || (Ri + Rgen)) / (β + 1) Small value, because divided by β +1.

The complete equation below for Rout,

Rout = R_C || (r_0 + Ref || [r_π + Rb || (Ri + Rgen)] / (β +1))

Because r_o is greater than 30kΩ we approximate Rout = Rc || "large" = Rc

Step CEwRef4.4: Current Gain
The current gain Ai can be obtained i_{load} and i_{in} or calculated from Av Rin and Rload.

$$\text{Ai} = \frac{Iload}{Iin} = \frac{Vout/_{Rload}}{Vin/_{Rin}} = \text{Av}\frac{\text{Rin}}{\text{Rload}}$$

Step CEwRef4.5: Power gain

G = Pout / Pin = Vout * Iload / Vin * Iin = Av * Ai
In decibels G_{dB} = 10log (Av * Ai)

Step CEwRef4.6: Vin and Voc of Vgen
Input signal level need to produce the required output voltage.
Vin = Vout / Av

The open circuit voltage of the generator to produce the required output voltage.
Because of Voltage divider because the output impedance of the Rgen = 50Ω

Vgen = Vin (Rgen + Rin) / Rin

Use this value in LTspice and the laboratory Function generator.

CEwRef Part 5: Frequency response with Ref

With the Q-point being set after the sequence of steps, we can go for the selection of capacitors and finally connect the signal generator at input and measure the output waveform.

Step CEwRef 5.1: Low frequency cut off. F_L

First we will select C_{in}, C_{out} and C_E which jointly would set the roll-off beyond the lower cut-off frequency. Set any frequency within the range as your lower cut-off frequency and let us call it f_L. Three capacitors will introduce 3 zeros in the transfer function of the system. Because we will set 3 zeros at the same frequency we must use the Band Width Shrinkage factor.

$$\text{BWshrinkage} = \sqrt{2^{\frac{1}{n}} - 1}$$

Where n is the number of zeros for low frequency breakpoints at same frequency.
The low frequency cutoff average of the individual time constants with shrinkage faction apllided be we have set all the time constants the same.

$$f_L = \frac{f_{C_{in}} + f_{C_{out}} + f_{C_E}}{3\sqrt{2^{\frac{1}{3}} - 1}}$$

Setting 3 frequencies equal, we get,

$f_{Cin} = f_{Cout} = f_{CE} = f_L \sqrt{2^{1/3} - 1}$

Find the C for each breakpoint f_{Cin} , f_{Cout} , and f_{CE} where n = 3.

$$\text{C} = \frac{1}{2\pi f_C \text{ (R seen by C)}}$$

Where C is the capacitor that sets the breakpoint f_C

R is the Thevenin equivalent resistance seen by the capacitor.

RemitterBase is the impedance looking in the BJT emitter to base.

RemitterbBase = $(r_\pi + Rb \parallel (Ri + Rgen)) / (\beta + 1)$ Small value

$R_{CE} = Reb \parallel (Ref + (ro + R_C \parallel R_{Load}) \parallel RemitterBase)$

Step CEwRef 5.2: High frequency cut off. F_H

C_{hi} Sets the higher cut-off frequency f_H which is to be set from the specified range.

In this case because Chi, and Ch2 are to the same break point. We must use the band shrinkage factor with n = 2. We need only to find a two poles at F_h / bandshrinage = $f_{chi} = f_{ch2}$ to set the high frequency cutoff.

Set Fchi = Fchi2 = Fh / $\sqrt{2^{1/2} - 1}$

Rb = Rb1 || Rb2 Base bias resistors

Rbase = r_π + (β + 1) (Ref || (ro + Rc || Rload)) Looking into the Base of the BJT.

Rin2 = Rb || Rbase

R seen by C_{hi} R_{Chi} = (Rgen + Ri) || Rin2

$$C_{hi} = \frac{1}{2\pi f_{Chi}\,(\text{R seen by } C_{hi})}$$

R seen by C_{hi2} R_{Chi2} = Rout || Rload Note: use the correct Rout depending on Ref

$$C_{hi2} = \frac{1}{2\pi f_{Chi2}\,(\text{R seen by } C_{hi2})}$$

The following table list the equivalent resistance expressions seen by the capacitors.

Rsig	Rgen+Ri
RemitterBase	(r_π + Rb || (Ri + Rgen)) / (β + 1)
C_{in}	Rsig + Rin2
Cout	RLoad + Rout
C_E	Reb || (Ref + (ro + R_C || R_{Load}) || RemitterBase)
C_{hi}	Rsig || Rin2
C_{hi2}	Rout || Rload

CEwRef Table 1: Resistance Seen By Capacitors

Section 3: Common Collector CC Amplifier Design

Vout is not inverted so the gain Av and Ai are positive.

Designing procedure of common collector BJT amplifier has three areas. First, we have to set the Q-point, which is the DC operating point. Since, there is no specification regarding the Q-point in the design requirements; it leaves the designer enough freedom to choose the operating point as necessary for the application. However, remember that the specifications are in terms of input and output impedance, gain, frequency response characteristics and peak output voltages ultimately restricts the Q-point in a narrow window. It is difficult to derive this point without some intelligent guess and the following steps would work out for the given conditions. We will start to choose a Q-point to allow maximum output voltage swing

For the Common Collector configuration, the circuit diagram shown in CC Figure 1. The small signal equivalent model in CC Figure 3.

For this configuration, same steps are involved for the calculation of Rb1, Rb2 and R_E with few minor changes. Note that R_C is absent in this case

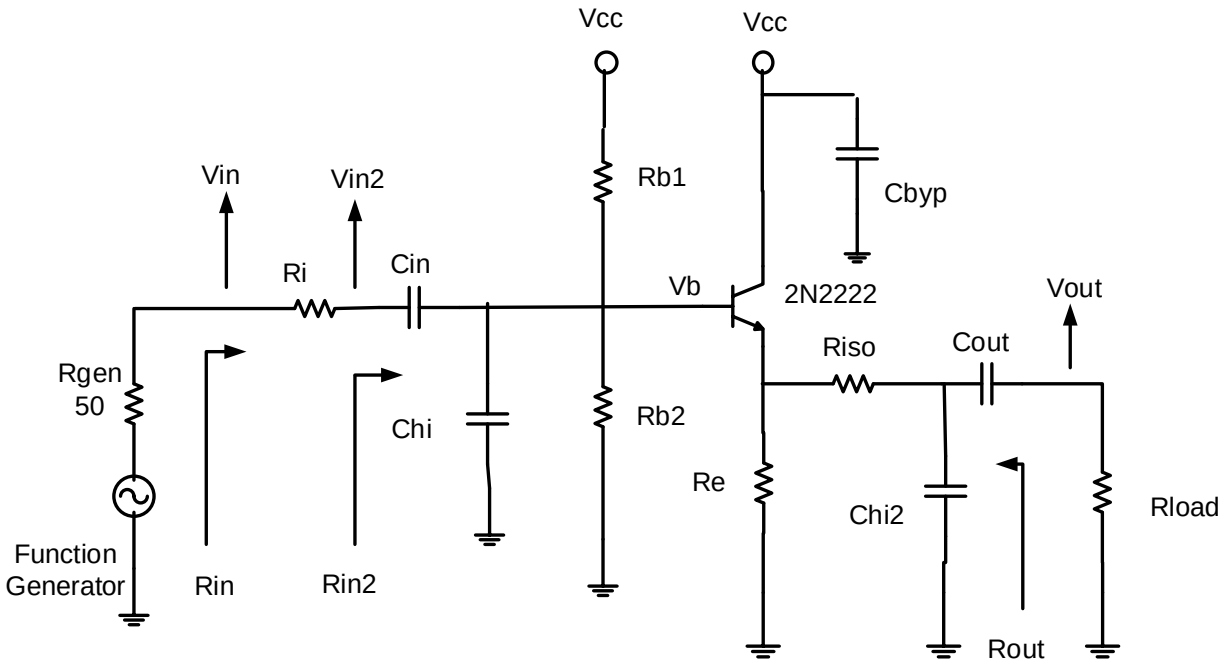
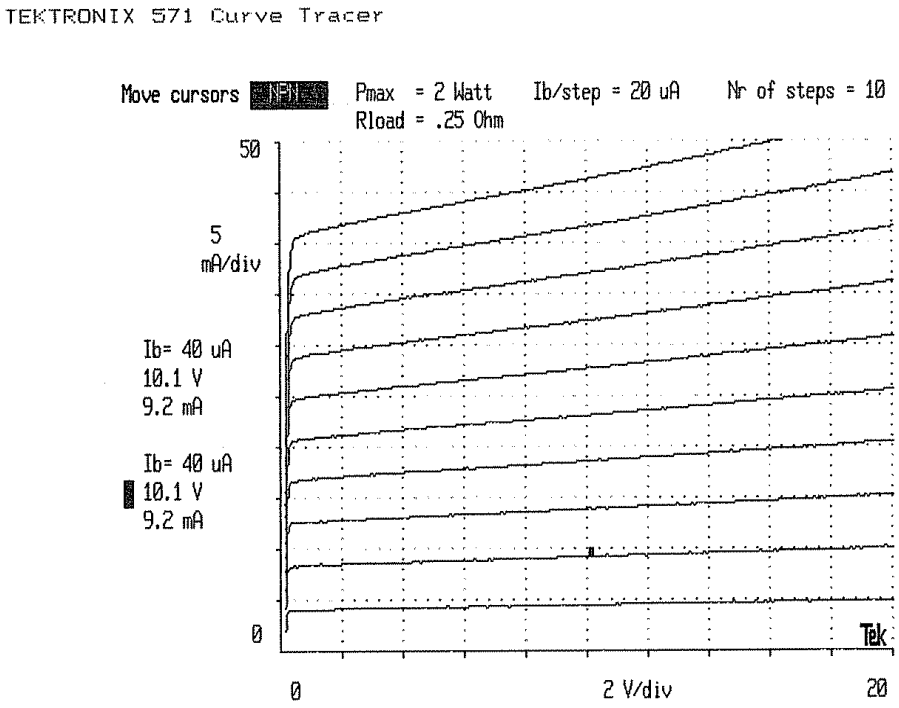


Figure 1: BJT Common Collector CC configuration



CC Figure 2: CC BJT curve.

CC Part 1: Measure the device parameters

Step CC1.1: We need to estimate a Q-point to find an estimate for ro and gm.

For the design of the amplifier, the 2 parameter values required are r_o and β. Derived from the transistor characteristics curve shown in CC Fig.2, one can set an approximate Q-point (V_{CE} and I_C) in the active region and measure ro and β. We will solve for V_{CE} and estimate I_C.

Solve for V_{CE} see below **Step CC2.1**. Use Vout peak to find I_{load} peak: Iload = Vout / Rload.

For an estimated I_C Q-point use $I_C \approx 2.6 * I_{load}$ peak this is not the solution to your design Q-point. We can use an estimated I_C because ro and β will not very much with small changes in Q-point.

ro = $\Delta V_{CE} / \Delta I_C$ the slope of a line thru the estimated Q-point

β = $\Delta I_C / \Delta I_B$ measured around the estimated Q-point

Plot the estimated Q-point (V_{CE}, I_C) on the BJT characteristics curve.
From the curves CC Fig. 2 estimate V_{CE}sat the point where the curve begins to flattens out ≈ 0.2 Vdc

CC Part 2: Find the Q-point

Step CC2.1: Derive V_E and V_{CE} Q- point

We will start with V_E(max) and V_E(min).

V_{CE}sat = 0.2V

VoutEmitter = Vout + I_{Load} * Riso The AC output voltage at the emitter.

V_E(max) = Vcc – V_{CE}sat – (VoutEmitter + 20%VoutEmitter)

V_E(min) = VoutEmitter + 20% VoutEmitter

V_E = (V_E(max) + V_E(min)) / 2 Midpoint V_E Q-point

V_{CE} = V_{CC} - V_E The V_{CE} Q-point

Step CC2.2: Now find the value of R_E and I_E

The DC equation: $V_E = R_E I_E$

The AC equation: VoutEmitter = i_e (R_E || r_o || (R_{Load} + Riso))

Rewrite: VoutEmitter = i_e R_E (r_o || (R_L + Riso))/ (R_E + (r_o || (R_L + Riso)) Parallel resistance equation

Substituting in $V_E = i_e R_E$

Combined equation: VoutEmitter = V_E (r_o || (R_{Load} + Riso)) / (R_E + (r_o || (R_{Load} + Riso))))

Solve for R_E; Add 20% VoutEmitter t so the collector current is not set to an edge.

$$R_E = \frac{V_E}{V_{outEmitter} + 20\% V_{outEmitter}} (r_o \parallel R_L + Riso) - (r_o \parallel R_L + Riso)$$ Rearranged combined equation

Calculate I_E, I_C, and r_π

$I_E = V_E / R_E$

Ic = I_E (β / (β + 1))

r_π = (β vt) / I_C rπ is base to emitter resistance Hybrid Pie model.

Where vt = kT/q at room temperature is vt ≈ 26mV.

CC Part 3: Find Rb1, and Rb2. (2 Methods)

Method 1.

(Do not use Method 1 for your design.) Use step CC3.2

Step CC3.1: Calculate Rb1, Rb1. Based on I_B

We will set the current in the base bias resisters Rb1, and Rb2 lower then 10*Ib from CE keep the Rin to a higher value.

Irb1 = 3*I_B and Irb2 = 2*I_B Current thru the base bias resistors
$V_B = V_E + V_{BE}$ Q - point values
Rb1 = (Vcc – Vb) / 3 I_B
Rb2 = Vb / 2 I_B

Rb = Rb1 || Rb2 Base bias resistors.

Method 2.
(Use this Method)

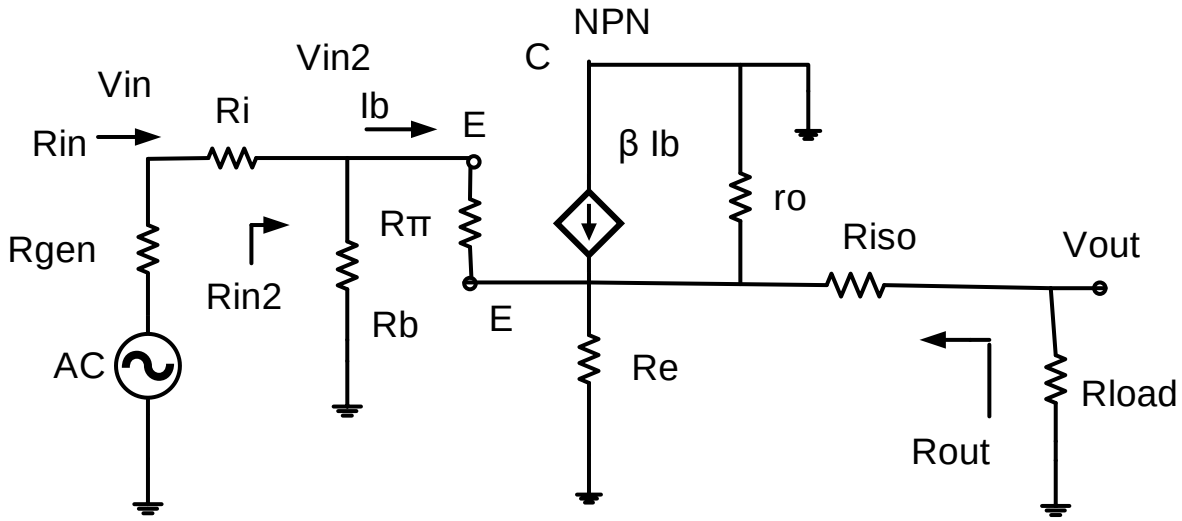
Step CC3.2: Calculate Rb1, and Rb2 Based on the requested Rin
Require Rin set to a given value. Need Vcc, Vb, r_π, ro, β, Re, Rload, and Ib.
Given Rin calculate Rin2.

Rin2 = Rin –Ri Solve Rin2 needed to Rin requirements.

Solve for Rb from Rin2 and Rbase.
Rbase = r_π + (β + 1) ((ro || R_E || (Riso + Rload))) Impedance looking into BJT base at midband.

Rb = 1 /((1 / Rin2) – (1 / Rbase)) Solve for Rb from Rin2, and Rbase to meet Rin requirements.

Find Rb1 first then Rb2
Rb1 = Vcc / ((Vb / Rb) + Ib) Solve for Rb1.
Rb2 = Vb / (((Vcc –Vb) /Rb1) –Ib) Solve Rb2 from Vb and current thru Rb2: Irb2 = Ir_{b1} – Ib



CC Figure 3: Small signal equivalent model for common collector model

CC Part 4: Calculate Rin, Rout, Av, and Ai

Step CC4.1: Input Impedance:

Rb = Rb1 || Rb2

Rbase = r_π + (β + 1) ((ro || R_E ||(Riso + Rload))) Impedance looking into BJT base.

Rin2 = Rb || Rbase

Rin = Rin2 + Ri Note: Ri is the resistor in the input used as a shunt to measure input current.

Step CC4.2: Output Impedance

RemitterBase is the impedance looking in the BJT emitter towards the base.

RemitterBase = (r_π + Rb || (Ri + Rgen)) / (β + 1)

Rout = (R_E || ro || RemitterBase) + Riso

Step CC4.3: Derivation of Av Voltage Gain

Av is positive: Vout is not inverted.

Referring to CC Fig.3, let us find Av = Vout / Vin which would be a key step in calculating Av.

Rbase = r_π + (β + 1) ((ro || R_E || (Riso + Rload))) Impedance looking into BJT base.

Rb = Rb1 || Rb2

Rin2 = Rb || Rbase

Rin = Ri + Rin2

RemitterBase = (r_π + Rb || (Ri + Rgen)) / (β + 1) Impedance looking into the BJT emitter towards the Base.

Rout = (R_E || ro || RemitterBase) + Riso

AC Voltage at the emitter.

AC voltage VoutEmitter = ie (RE || ro || (Riso + Rload))

AC voltage VoutEmitter = (β + 1) ib (RE || ro || (Riso + Rload))

Voltage across the load resistor Vout = VoutEmitter * (Rload / (Rload +Riso))

AC voltage Vout = (β + 1) i_b (R_E || ro || (Riso + Rload)) * (Rload / (Rload +Riso))

AC Voltage at the function generator Vin = Vin2 (Rin / Rin2)

AC Voltage at the base Vin2 = V_{BE} + VoutEmitter

Vin2 = Rπ i_b + i_b (β +1) (R_E || ro || (Rload + Riso)) = i_b (Rπ + (β+1) (Rs || ro || (Rload +Riso)))

Av2 = Vout / Vin2 = (β+ 1) i_b (R_E || ro || (Rload + Riso)) / i_b (Rπ + (β+1) (R_E || ro || (Rload + Riso)))

Vin = Vin2 (Rin / Rin2) Voltage divider Vin to Vin2

Need Vout to find Av.

Vout = VoutEmitter * (Rload / (Rload +Riso)) Voltage divider VoutEmitter to Vout

Or rewriting VoutEmitter = Vout * ((Rload +Riso) / Rload) Find VoutEmitter from Vout.

Av = Vout / Vin = (Rin2 / Rin) (Rload /(Rload + Riso)) (β+ 1) i_b (R_E || ro || (Rload + Riso)) / i_b (Rπ + (β+1) (R_E || ro || (Rload + Riso)))

Canceling out i_b and including the factor for Vin2 to Vin gives

This is the final equation for Av = Vout / Vin Av is positive: Vout is not inverted

Calculation of the Av.

Av = (Rin2 / Rin) (Rload /(Rload + Riso)) (β + 1) (R_E || ro || (Rload + Riso)) / (Rπ + (β+1) (R_E || ro || (Rload + Riso)))

Thus, the voltage gain should be close to 1. Hence, the output follows the input. So, the Common Collector configuration is also known as an Emitter follower.

Step CC4.4: Calculation of the Ai Current Gain

$$\mathrm{Ai} = \frac{Iload}{Iin} = \frac{Vout/_{Rload}}{Vin/_{Rin}} = \mathrm{Av}\frac{\mathrm{Rin}}{\mathrm{Rload}}$$

Step CC4.5: Power gain

G = Pout / Pin = Vout * Iload / Vin * Iin = Av * Ai
In decibels G_{dB} = 10log (Av * Ai)

Step CC4.6: Vin and Voc of Vgen
Input signal level need to produce the required output voltage.
Vin = Vout / Av

The open circuit voltage of the generator to produce the required output voltage.
Because of Voltage divider because the output impedance of the Rgen = 50Ω

Vgen = Vin (Rgen + Rin) / Rin

Use this value in LTspice and the laboratory Function generator.

CC Part 5: Frequency response.

The capacitor values can be calculated as before (CE amp), the only difference being *n* = 2 for low pass calculations since we are using two capacitors instead of 3.
With the Q-point being set after the sequence of steps, we can go for the selection of capacitors and finally connect the signal generator at input and measure the output amplified waveform.

Step CC5.1: Low frequency cut off. F_L

First we will select C_{in}, and C_{out} which jointly would set the roll-off beyond the lower cut-off frequency. Set any frequency within the range as your lower cut-off frequency and let us call it f_L. Two capacitors will introduce 2 zeros in the transfer function of the system. Because we will set 2 pole at the same frequency we must use the Band Width Shrinkage factor.

$$\text{BWshrinkage} = \sqrt{2^{\frac{1}{n}} - 1} \qquad n = 2$$

Where n is the number of zeros for low frequency breakpoints at same frequency.
Setting 2 frequencies equal, we will, multiply the F_L by the Band Width Shrinkage factor

$f_{Cin} = f_{Cout} = f_L \sqrt{2^{1/2} - 1}$

Find the C for each breakpoint f_{Cin} , and f_{Cout} , where n = 2.

$$C = \frac{1}{2\pi f_C \,(\text{R seen by C})}$$

Where C is the capacitor that sets the breakpoint f_{Cin}, and f_{Cout}

R is the Thevenin equivalent resistance seen by the capacitor.

Step CC 5.2: High frequency cut off. F_H

Chi, and Chi2 on the contrary, sets the high cut-off frequency f_H which is to be set from the specified range. Where n = 2 the number of high frequency break points at the same frequency.

In this case because Chi, and Ch2 are set to the same break point. We must use the band shrinkage factor with n = 2. We need only to find a two poles at F_h / bandshrinage = $f_{chi} = f_{ch2}$ to set the high frequency cutoff.

Setting the 2 high frequencies break point equal, we will, divide the Fh (high frequency cutoff desired) by the Band Width Shrinkage factor

Set Fchi = Fchi2 = Fh / $\sqrt{2^{1/2} - 1}$

Rbase = r_π + ((β + 1) * (ro || R_E || (Rload + Riso))) Impedance looking into BJT base.

Rb = Rb1 || Rb2

Rin2 = Rb || Rbase

R seen by C_{hi} R_{Chi} = (Rgen + Ri) || Rin2

$$C_{hi} = \frac{1}{2\pi f_{Chi}\,(\text{R seen by } C_{hi})}$$

R seen by C_{hi2} R_{Chi2} = Rout || Rload

$$C_{hi2} = \frac{1}{2\pi f_{Chi2}\,(\text{R seen by } C_{hi2})}$$

The following table enlists the particular expressions.

Thevenin equivalent resistance seen by the capacitor.

Rsig	Rgen+Ri
C_{in}	Rsig + Rin2
Cout	R_{Load} + Rout
Chi	Rsig || Rin2
Chi2	Rout || Rload

CC Table 1: Resistance Seen By Capacitors