

**Vout is not inverted so the gains Av and Ai are positive.**

Designing procedure of common collector BJT amplifier has three areas. First, we have to set the Q-point, which is the DC operating point. Since, there is no specification regarding the Q-point in the design requirements; it leaves the designer enough freedom to choose the operating point as necessary for the application. However, remember that the specifications are in terms of input and output impedance, gain, frequency response characteristics and peak output voltages ultimately restricts the Q-point in a narrow window. It is difficult to derive this point without some intelligent guess and the following steps would work out for the given conditions. We will start to choose a Q-point to allow maximum output voltage swing

For the Common Collector configuration, the circuit diagram shown in CC Figure 1. The small signal equivalent model in CC Figure 3.

For this configuration, same steps are involved for the calculation of Rb1, Rb2 and Re with few minor changes. Note that Rc is absent in this case.

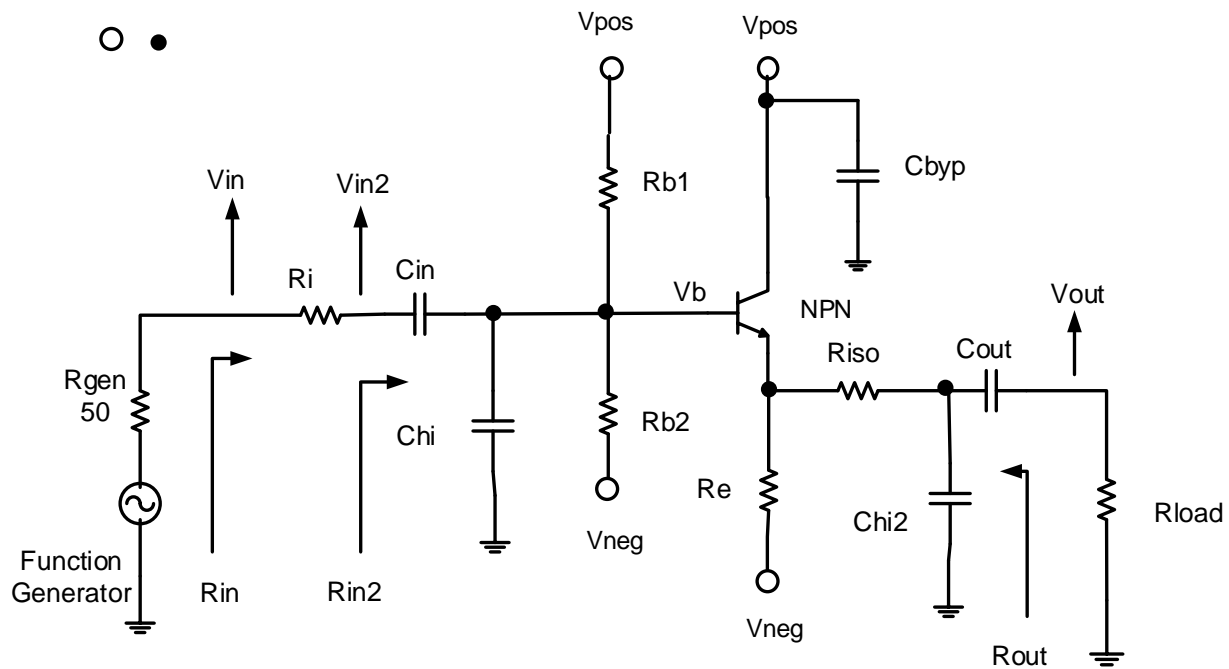


Figure 1: BJT Common Collector CC configuration

## CC Part 1: Measure the device parameters use CC Figure 2

Measure transistor parameters  $I_{Cest}$ ,  $V_{CEsat}$ ,  $\beta_{DC}$ ,  $\beta_{AC}$ ,  $V_E$ ,  $V_{CE}$ ,  $\beta_{AC}$ ,  $\beta_{DC}$ ,  $r_o$ , and  $r_{\pi}$

**Step CC 1.1:** Estimate the  $I_C$  collector current Q-point use  $I_C$  estimate  $\approx 2.6 * I_{load}$  peak this is not the solution to your design Q-point. We can use an estimated  $I_C$  because  $r_o$  and  $\beta$  will not change very much with small changes in Q-point

**Step CC 1.2:** The saturated  $V_{ce}$  voltage  $V_{CE-sat}$ : From the curves CC Fig. 2 estimate  $V_{CEsat}$  the point where the curve begins to flattens out  $\approx 0.2$  Vdc

**Step CC 1.3:** Calculate the midpoint  $V_E$  and  $V_{CE}$  : **Step CC 2.1**

**Step CC 1.4:** Find  $r_o$ ,  $\beta_{AC}$ ,  $\beta_{DC}$ , and  $r_{\pi}$ : Step CEwRef 1.5

$r_o = \Delta V_{CE} / \Delta I_C$  the slope of a  $I_B$  curve near the Q-point.

$\beta_{AC} = \Delta I_C / \Delta I_B$  measured around Q-point est.

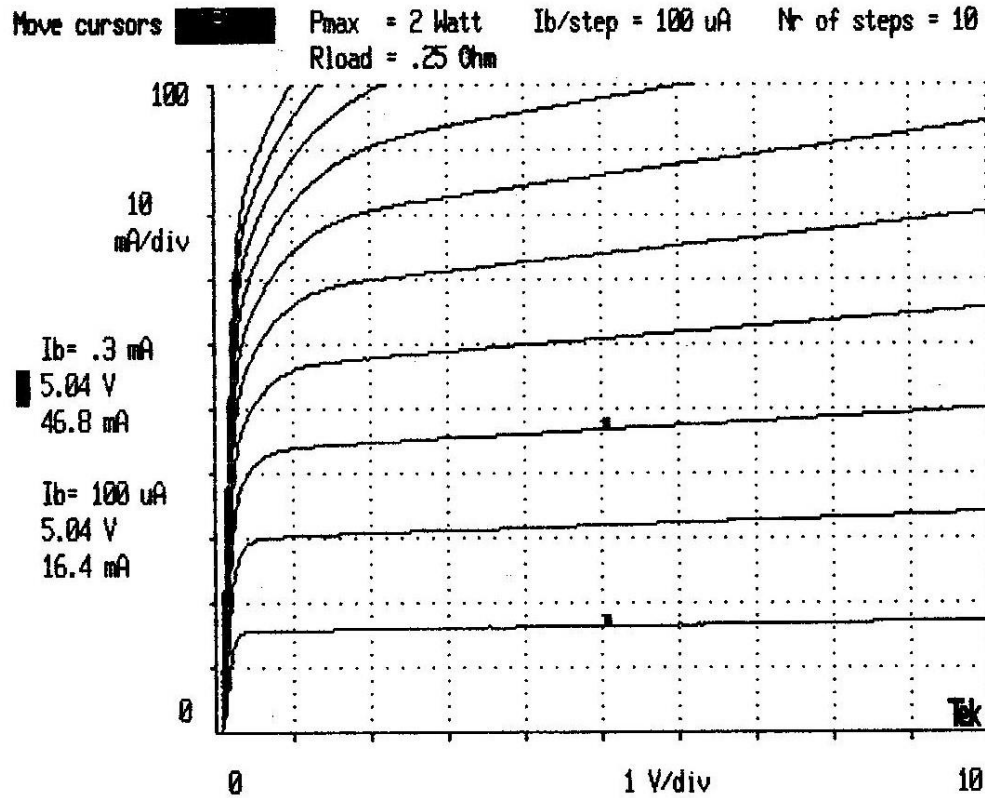
$\beta_{DC} = I_C / I_B$  measured around Q-point est

$r_{\pi} = (\beta_{DC} V_T) / I_C$   $r_{\pi}$  is base to emitter resistance of the Hybrid Pie model.

Where  $V_T = kT/q$  at room temperature is  $V_T \approx 26$ mV.

Plot the estimated Q-point ( $V_{CE}, I_C$ ) on the BJT characteristics curve.

**Note: If the equation has Just  $\beta$  the use  $\beta_{AC}$ .**



CC Figure 2: CC BJT curve. The first curve is  $I_B = 100\mu A$

**X axis is  $V_{CE}$ , Y axis is  $I_C$**

To find which  $I_B$  curve you are on count from a known curve (First  $I_B$  curve  $I_B = 5\mu A$ ) by the step size at the top of the curve label step =  $5\mu A$ .

**$r_o = \Delta V_{CE} / \Delta I_C$**  Where  $V_{CE}$  is the X Axis. We do not want to start at zero because the first part of the curve is nonlinear we want to use the area where the curve is linear. So chose  $V_{CE}$  between 1V to 10V therefore  $\Delta V_{CE} = 10V - 1V = 9V$ . Where  $I_C$  is the Y Axis. We pick an  $I_B$  curve close to our estimated or actual Q-Point and measure the current  $I_C$ :1 at two points along the  $I_B$  curve at  $V_{CE} = 1V$  the second  $I_C$ : 2 current at  $V_{CE} = 10V$   $\Delta I_C = I_C:2 - I_C:1 = 0.3mA$  The calculation of  $r_o$  at the chosen  $I_B$  curve  **$r_o = \Delta V_{CE} / \Delta I_C$**

**$\beta_{AC} = \Delta I_C / \Delta I_B$**  at the  $V_{CE}$  (from step **CC 1.3**) on the X-Axis find the  $\Delta I_B$  which is the current  $I_B$  between the two  $I_B$  curves on both sides of the Q-Point. Where the two  $I_C$  the currents associated with the two points on the  $I_B$  curves at  $V_{CE}$ .

$\beta_{DC} = I_C / I_B$  at the  $V_{CE}$  (from step **CC 1.3:** ) on the X-Axis find the  $I_B$  which is the current  $I_B$  form the curves closes to the Q-Point. Where the  $I_C$  the currents associated with the point on the  $I_B$  curves at  $V_{CE}$ .

## CC Part 2: Find the Q-point

### Step CC2.1: Derive $V_E$ and $V_{CE}$ Q- point

We will start with  $V_E(\max)$  and  $V_E(\min)$ .

$$V_{CESat} = 0.2V$$

$V_{BE} = 0.7V_{dc}$  Use the higher value because the Base and Collector current is higher buffer stage.

$V_{outEmitter} = V_{out} + I_{Load} * R_{iso}$  The AC output voltage at the emitter.

$$V_E(\max) = V_{CC} - V_{CESat} - (V_{outEmitter} + 20\%V_{outEmitter})$$

$$V_E(\min) = V_{ee} + V_{outEmitter} + 20\% V_{outEmitter}$$

$$V_E = (V_E(\max) + V_E(\min)) / 2 \quad \text{Midpoint } V_E \text{ Q-point}$$

$$V_C = V_{CC}$$

$$V_{CE} = V_C - V_E \quad \text{The } V_{CE} \text{ Q-point}$$

### Step CC2.2: Now find the value of $R_e$ and $I_E$

The DC equation:  $(V_E - V_{ee}) = R_e * I_E$

The AC equation:  $V_{outEmitter} = i_e ( R_e \parallel r_o \parallel (R_{Load} + R_{iso}) )$

Rewrite:  $V_{outEmitter} = i_e R_e ( r_o \parallel ( R_L + R_{iso} ) ) / ( R_e + ( r_o \parallel ( R_L + R_{iso} ) ) )$  Parallel resistance equation

Substituting in  $(V_E - V_{ee}) = i_e R_e$

Combined equation:  $V_{outEmitter} = (V_E - V_{ee})(r_o \parallel (R_{Load} + R_{iso})) / (R_e + (r_o \parallel (R_{Load} + R_{iso})))$

Solve for  $R_e$ ; Add 20%  $V_{outEmitter}$  t so the collector current is not set to an edge.

$$R_e = \frac{V_E - V_{ee}}{V_{outEmitter} + 20\%V_{outEmitter}} (r_o \parallel (R_L + R_{iso})) - (r_o \parallel (R_L + R_{iso})) \quad \text{Rearranged combined equation}$$

Calculate  $I_E$ ,  $I_C$ , and  $r_{\pi}$

$$I_E = (V_E - V_{ee}) / R_e$$

$$I_C = I_E (\beta_{DC} / (\beta_{DC} + 1))$$

$r_{\pi} = (\beta_{DC} v_t) / I_C$   $r_{\pi}$  is base to emitter resistance Hybrid Pie model.

Where  $v_t = kT/q$  at room temperature is  $v_t \approx 26mV$ .

### CC Part 3: Find Rb1, and Rb2. (2 Methods)

#### Method 1.

(Do not use Method 1 for your design.) Use step CC3.2

#### Step CC3.1: Calculate Rb1, Rb2. Based on $I_B$

We will set the current in the base bias resistors Rb1, and Rb2 lower than  $10 \cdot I_B$  from the CE amplifier keep the Rin to a higher value.

$I_{Rb1} = 3 \cdot I_B$  and  $I_{Rb2} = 2 \cdot I_B$  Current thru the base bias resistors

$V_B = (V_E) + V_{BE}$  Q - point values

$R_{b1} = (V_{CC} - V_B) / 3 I_B$

$R_{b2} = (V_B - V_{EE}) / 2 I_B$

$R_b = R_{b1} \parallel R_{b2}$  Base bias resistors.

#### Method 2.

(Use this Method)

#### Step CC3.2: Calculate Rb1, and Rb2 Based on the requested Rin

Require Rin set to a given value. Need  $V_{CC}$ ,  $V_B$ ,  $r_{\pi}$ ,  $r_o$ ,  $\beta$ ,  $R_E$ ,  $R_{load}$ , and  $I_B$ .

Given Rin calculate Rin2.

$V_B = V_E + V_{BE}$  Q - point values

$I_B = I_C / \beta_{DC}$

$R_{in2} = R_{in} - R_i$  Solve Rin2 needed to Rin requirements.

Solve for Rb from Rin2 and Rbase.

$R_{base} = r_{\pi} + (\beta_{DC} + 1) ((r_o \parallel R_E \parallel (R_{iso} + R_{load})))$  Impedance looking into BJT base at midband.

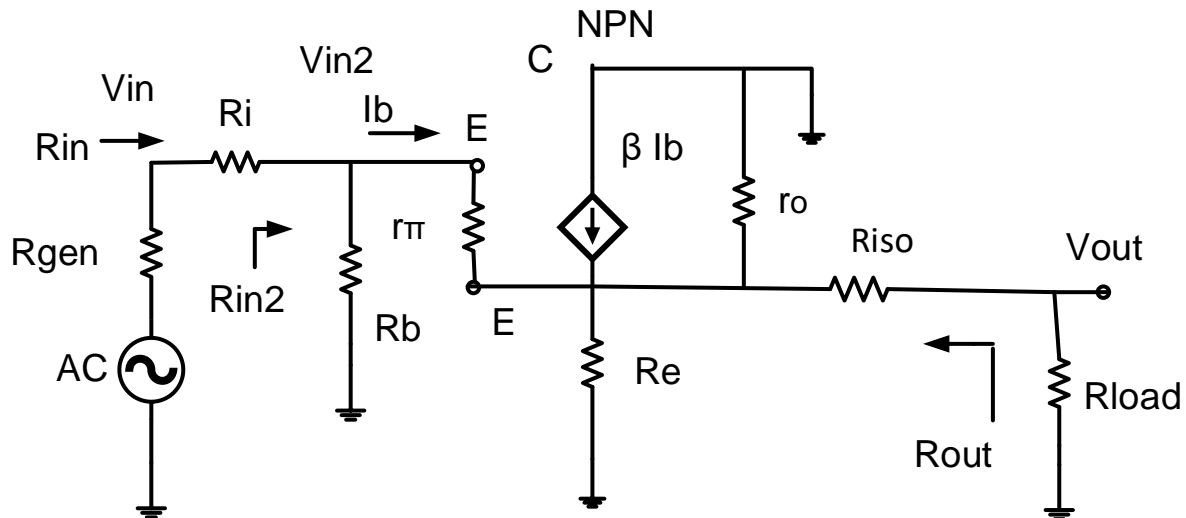
$R_b = 1 / ((1 / R_{in2}) - (1 / R_{base}))$  Solve for Rb from Rin2, and Rbase to meet Rin requirements.

Find Rb1 first then Rb2

$$R_{b1} = (V_{CC} - V_{ee}) / (((V_B - V_{ee}) / R_b) + I_B) \text{ Solve for } R_{b1}.$$

Solve  $R_{b2}$  from  $V_B$  and current thru  $R_{b2}$ :  $I_{R_{b2}} = I_{R_{b1}} - I_B$

$$R_{b2} = (V_B - V_{ee}) / (((V_{CC} - V_B) / R_{b1}) - I_B)$$



CC Figure 3: Small signal equivalent model for common collector model

#### CC Part 4: Calculate $R_{in}$ , $R_{out}$ , $A_v$ , and $A_i$

##### Step CC4.1: Input Impedance:

$$R_b = R_{b1} || R_{b2}$$

$R_{base} = r_{\pi} + (\beta + 1) ((r_o || R_e || (R_{iso} + R_{load})))$  Impedance looking into BJT base.

$$R_{in2} = R_b || R_{base}$$

$R_{in} = R_{in2} + R_i$  Note:  $R_i$  is the resistor in the input used as a shunt to measure input current.

##### Step CC4.2: Output Impedance

$R_{emitterBase}$  is the impedance looking in the BJT emitter towards the base.

$$R_{emitterBase} = (r_{\pi} + R_b || (R_i + R_{gen})) / (\beta + 1)$$

$$R_{out} = (R_e || r_o || R_{emitterBase}) + R_{iso}$$

The CC amplifier is known as a **Buffer Amplifier** because lower output impedance.

### Step CC4.3: Derivation of Av Voltage Gain

**Av is positive: Vout is not inverted.**

Referring to CC Fig.3, let us find  $A_v = V_{out} / V_{in}$  which would be a key step in calculating  $A_v$ .

$R_{base} = r_{\pi} + (\beta + 1) ((r_o \parallel R_E \parallel (R_{iso} + R_{load})))$  Impedance looking into BJT base.

$R_b = R_{b1} \parallel R_{b2}$

$R_{in2} = R_b \parallel R_{base}$

$R_{in} = R_i + R_{in2}$

$R_{emitterBase} = (r_{\pi} + R_b \parallel (R_i + R_{gen})) / (\beta + 1)$  Impedance looking into the BJT emitter towards the Base.

$R_{out} = (R_e \parallel r_o \parallel R_{emitterBase}) + R_{iso}$

AC Voltage at the emitter.

AC voltage  $V_{outEmitter} = i_e (R_e \parallel r_o \parallel (R_{iso} + R_{load}))$

AC voltage  $V_{outEmitter} = (\beta + 1) i_b (R_e \parallel r_o \parallel (R_{iso} + R_{load}))$

Voltage across the load resistor  $V_{out} = V_{outEmitter} * (R_{load} / (R_{load} + R_{iso}))$

AC voltage  $V_{out} = (\beta + 1) i_b (R_e \parallel r_o \parallel (R_{iso} + R_{load})) * (R_{load} / (R_{load} + R_{iso}))$

AC Voltage at the function generator  $V_{in} = V_{in2} (R_{in} / R_{in2})$

AC Voltage at the base  $V_{in2} = V_{BE} + V_{outEmitter}$

$V_{in2} = r_{\pi} i_b + i_b (\beta + 1) (R_e \parallel r_o \parallel (R_{load} + R_{iso})) = i_b (r_{\pi} + (\beta + 1) (R_e \parallel r_o \parallel (R_{load} + R_{iso})))$

$A_{v2} = V_{out} / V_{in2} = (\beta + 1) i_b (R_e \parallel r_o \parallel (R_{load} + R_{iso})) / i_b (r_{\pi} + (\beta + 1) (R_e \parallel r_o \parallel (R_{load} + R_{iso})))$

$V_{in} = V_{in2} (R_{in} / R_{in2})$  Voltage divider  $V_{in}$  to  $V_{in2}$

Need  $V_{out}$  to find  $A_v$ .

$V_{out} = V_{outEmitter} * (R_{load} / (R_{load} + R_{iso}))$  Voltage divider  $V_{outEmitter}$  to  $V_{out}$

Or rewriting  $V_{outEmitter} = V_{out} * ((R_{load} + R_{iso}) / R_{load})$  Find  $V_{outEmitter}$  from  $V_{out}$ .

$A_v = V_{out} / V_{in} = (R_{in2} / R_{in}) (R_{load} / (R_{load} + R_{iso})) (\beta + 1) i_b (R_e \parallel r_o \parallel (R_{load} + R_{iso})) / i_b (r_{\pi} + (\beta + 1) (R_e \parallel r_o \parallel (R_{load} + R_{iso})))$

Canceling out  $i_b$  and including the factor for  $V_{in2}$  to  $V_{in}$  gives

**This is the final equation for  $A_v = V_{out} / V_{in}$   $A_v$  is positive:  $V_{out}$  is not inverted**

**Calculation of the  $A_v$ .**

**$A_v = (R_{in2} / R_{in}) (R_{load} / (R_{load} + R_{iso})) (\beta + 1) (R_E \parallel r_o \parallel (R_{load} + R_{iso})) / (r_{\pi} + (\beta + 1) (R_e \parallel r_o \parallel (R_{load} + R_{iso})))$**

Thus, the voltage gain should be close to 1. Hence, the output follows the input. So, the Common Collector configuration is also known as an Emitter follower.

#### Step CC4.4: Calculation of the Ai Current Gain

$$A_i = \frac{I_{load}}{I_{in}} = \frac{V_{out}/R_{load}}{V_{in}/R_{in}} = A_v \frac{R_{in}}{R_{load}}$$

#### Step CC4.5: Power gain

$$G = P_{out} / P_{in} = V_{out} * I_{load} / V_{in} * I_{in} = A_v * A_i$$

$$\text{In decibels } G_{dB} = 10 \log ( A_v * A_i )$$

#### Step CC4.6: Vin and Voc of Vgen

Input signal level need to produce the required output voltage.

$$V_{in} = V_{out} / A_v$$

The **open circuit voltage** of the generator to produce the required output voltage. Because of Voltage divider because the output impedance of the Rgen = 50Ω

$$V_{gen} = V_{in} (R_{gen} + R_{in}) / R_{in}$$

Use this value in LTspice and the laboratory Function generator.

#### CC Part 5: Frequency response.

The capacitor values can be calculated as before (CE amp), the only difference being  $n = 2$  for low pass calculations since we are using two capacitors instead of 3.

With the Q-point being set after the sequence of steps, we can go for the selection of capacitors and finally connect the signal generator at input and measure the output amplified waveform.

#### Step CC5.1: Low frequency cut off. $F_L$

First we will select  $C_{in}$ , and  $C_{out}$  which jointly would set the roll-off beyond the lower cut-off frequency. Set any frequency within the range as your lower cut-off frequency and let us call it  $f_L$ . Two capacitors will introduce 2 zeros in the transfer function of the system. Because we will set 2 pole at the same frequency we must use the Band Width Shrinkage factor.

$$BW_{shrinkage} = \sqrt{2^{\frac{1}{n}} - 1} \quad n = 2$$

Where n is the number of zeros for low frequency breakpoints at same frequency.

Setting 2 frequencies equal, we will, multiply the  $F_L$  by the Band Width Shrinkage factor

$$\text{Set each break point to } F_{Cin} = F_{Cout} = F_L \sqrt{2^{1/2} - 1}$$

Find the C for each breakpoint  $f_{Cin}$ , and  $f_{Cout}$ , where  $n = 2$ .



$$C = \frac{1}{2\pi f_C (R \text{ seen by } C)}$$

Where C is the capacitor that sets the breakpoint  $f_{Cin}$ , and  $f_{Cout}$

R is the Thevenin equivalent resistance seen by the capacitor.

**Step CC 5.2:** High frequency cut off.  $F_H$

$Chi$ , and  $Chi2$  on the contrary, sets the high cut-off frequency  $f_H$  which is to be set from the specified range. Where  $n = 2$  the number of high frequency break points at the same frequency.

In this case because  $Chi$ , and  $Ch2$  are set to the same break point. We must use the band shrinkage factor with  $n = 2$ . We need only to find a two poles at  $F_h / \text{bandshrinkage} = f_{chi} = f_{ch2}$  to set the high frequency cutoff.

Setting the 2 high frequencies break point equal, we will, divide the  $F_h$  (high frequency cutoff desired) by the Band Width Shrinkage factor

$$\text{Set each break point to } F_{chi} = F_{chi2} = F_h / \sqrt{2^{1/2} - 1}$$

$R_{base} = r_{\pi} + ((\beta + 1) * (r_o \parallel R_e \parallel (R_{load} + R_{iso})))$  Impedance looking into BJT base.

$$R_b = R_{b1} \parallel R_{b2}$$

$$R_{in2} = R_b \parallel R_{base}$$

$$R \text{ seen by } C_{hi} \quad R_{chi} = (R_{gen} + R_i) \parallel R_{in2}$$

$$C_{hi} = \frac{1}{2\pi f_{chi} (R \text{ seen by } C_{hi})}$$

$$R \text{ seen by } C_{hi2} \quad R_{chi2} = R_{out} \parallel R_{load}$$

$$C_{hi2} = \frac{1}{2\pi f_{chi2} (R \text{ seen by } C_{hi2})}$$

The following table enlists the particular expressions.

Thevenin equivalent resistance seen by the capacitor.

$R_{sig}$	$R_{gen} + R_i$
$C_{in}$	$R_{sig} + R_{in2}$
$C_{out}$	$R_{Load} + R_{out}$
$Chi$	$R_{sig} \parallel R_{in2}$
$Chi2$	$R_{out} \parallel R_{load}$

CC Table 1: Resistance Seen By Capacitors