ClassB and ClassAB amplifier Design

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When the input signal is positive, the NPN transistor Q1 turns ON, the PNP transistor Q2 is OFF, and the output voltage is positive. The NPN transistor (emitter follower) is sourcing (pushing) the current into the load resistor during the positive cycle of the input voltage.
When the input signal is negative, the PNP transistor Q2 turns ON, the NPN transistor Q1 is OFF, and the output voltage is negative. The PNP transistor (emitter follower) is sinking (pulling) the current from the load resistor during the negative cycle of the input voltage.
This were it gets its name Push Pull stage. Design for the positive half (NPN) duplicate for the negative half (PNP).

Part 0: ClassB-AB For both ClassB and ClassAB

Step ClassB-AB 0.1: Find ro, and β For both ClassB and ClassAB

Find ro, and β from the **2N3904, 2N3906 characteristic curves (used for both**). Use for both NPN and PNP calculate at peak values $I_C \approx I_{load}$, and Vce = Vcc – Vout.

Use βMin = 100 for calculating **bias** (worse case). **This is the largest base current $I_B = I_C / \beta$**

Use β_{AC} from curves to calculate gain A_V, frequency response (capacitors), Rin, and Rout.

Step: ClassB-AB 0.2: Convert power in load to Vout peak and Iload peak

Solve for the Peak values of Vout, and Iload. You need the peak values to design the bias circuit to prevent saturation or cutoff. Goto **Step: ClassB-AB 0.25: if given Vout peak.0**

First step for lab is calculate Vout peak and Iload peak from the given Road, and Pload (power in load).

From the power equations, we get rms **values of current Iload and voltages Vout.**

Pload = (Vout rms)^2 / Rload

Solve for (Vout rms)^2 = Pload / Rload

Take square root of V^2 to find V **Vout** rms **= sqrt (Rload * Pload).**

Now convert Vout rms to Vout peak: **Vout** peak **= Vout** rms ***** **sqrt (2).**

Step: ClassB-AB 0.25: Start here if giver Vout peak.

VoutMax = Vout peak **+ 20% Vout** peak

Iload RMS = Vout RMS / Rload .

Solve for Iload peak

Iload peak = Vout peak / Rload

IloadMax = VoutMax / Rload

IcMax = IloadMax * βmin / (βmin +1)

Step: ClassB-AB 0.3: Find approximant Q-Point on the curves ClassAB Re1, Re2 are not known yet so ignore the voltage drop across Re1 there for Ve ≈ Vout for the finding of Q-Point on curves.

Because of the higher collector current VceSat we will use 1Vdc.VceSat = 1Vdc

Remember Vc = Vcc, and VoutMin = 0V

VceMin = Vcc – VoutMax. This at Vc = Vcc, Ve = VoutMax includes the 20%

VceMax= Vcc – VceSat – Voutmin Note: VoutMin = 0V the PNP transistor is off.

Use VceMax on the x-axis.

IloadMax = (Vout peak +20% Vout peak) / Rload   Do not design for an edge.

IeMax = IloadMax

IcMax = IeMax * βmin / (βmin +1)

Use IcMax on the y-axis or as close as you can on the curves.

Step ClassB-A 0.4: Find ro and β_{AC} and β_{DC} from curvers

For the Q-point on curves use IcMax, VceMax

Find ro and β_{AC} and β_{DC}. Use β_{Min} =100

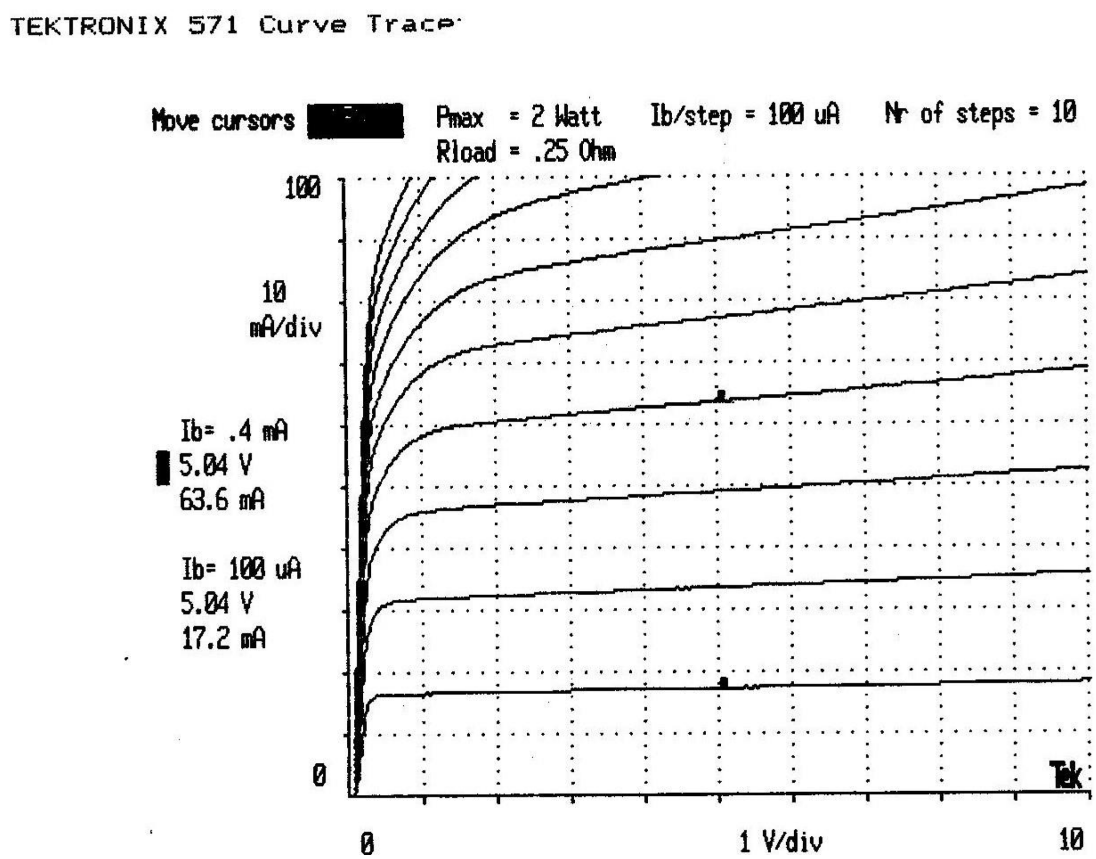

Figure 1 Class B AB. Curves for 2N3904 and 2N3906.

This section is the design of the Class B push pull amplifier.

Section: 1 Class B push pull stage.

Part 1 Class B

Step ClassB 1.1: ClassB Intro

Vdd = - Vee **Need both supplies equal but opposite with center ground.**

Vin2 = Vout – Vbe   Vin2 is the AC signal at the base of the BJT. Start from Vout.

Rin2 is the impedance looking into amplifier thru the Cin capacitor.

Vin = Vin2 (Ri + Rin2) / Rin2   **Ac input signal voltage** If you start at Vout to Vin2

Vin2 = Vin (Rin2 / (Rin2 + Ri))   **AC signal on the base**. If you start at Vin.

The output voltage can be expressed as

For |Vin| > Vbe (Ri + Rin2) / Rin2   Vout = vb - Vbe   **where Vbe = 0.7V DC bias vb is the AC signal on the base**.

For |Vin| < Vbe (Ri + Rin2) / Rin2   Vout = 0V **No output when input bellow | 0.7v |.**

At maximum Vout the gain Av2 = (Vin2 – Vbe) / Vout and Vin2 = Vin (Rin2 / (Rin2 + Ri))

Note: Av changes with Vin values.

Where Vout = Vin2 – Vbe   Note Vin2 is the ac signal on the base.

Therefor the Av changes with Vin signal

We design the positive half (NPN) and copy the values to the negative half (PNP).

Use the curves for 2N3906 (PNP) for 2N3904 (NPN) they both have the same characteristics but just opposite polarity. Use β_{min} = 100

Using the value of the **output voltage peak** during the positive cycle for the NPN transistor. We will design Rb1 = Rb2. The base bias resistors Rb1, and Rb2 are not required for the ideal case, but will we add them to hold both base voltages (**Q1, Q2**) to zero with Vin = 0.

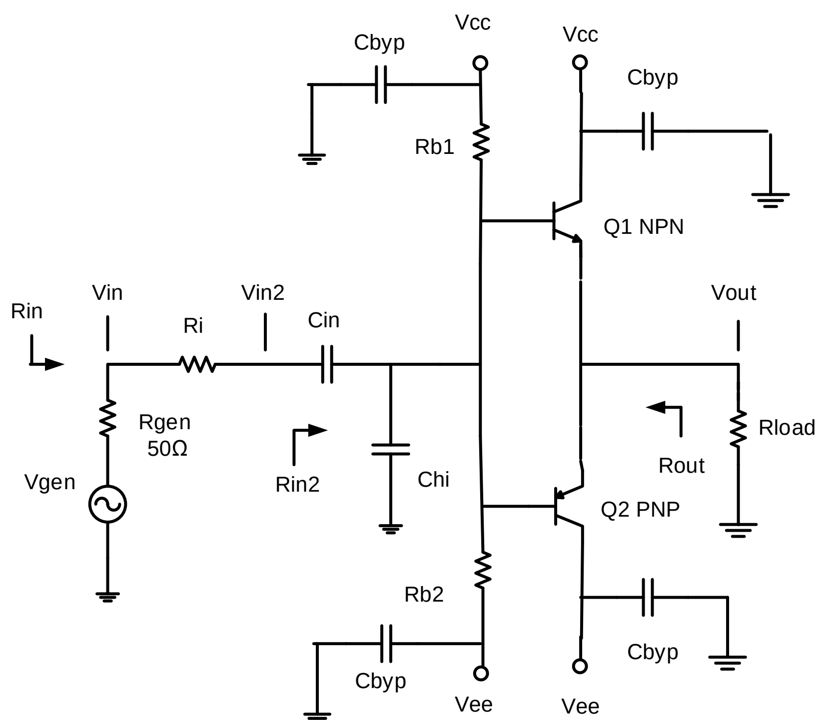

Figure 2. Class B. Push pull stage

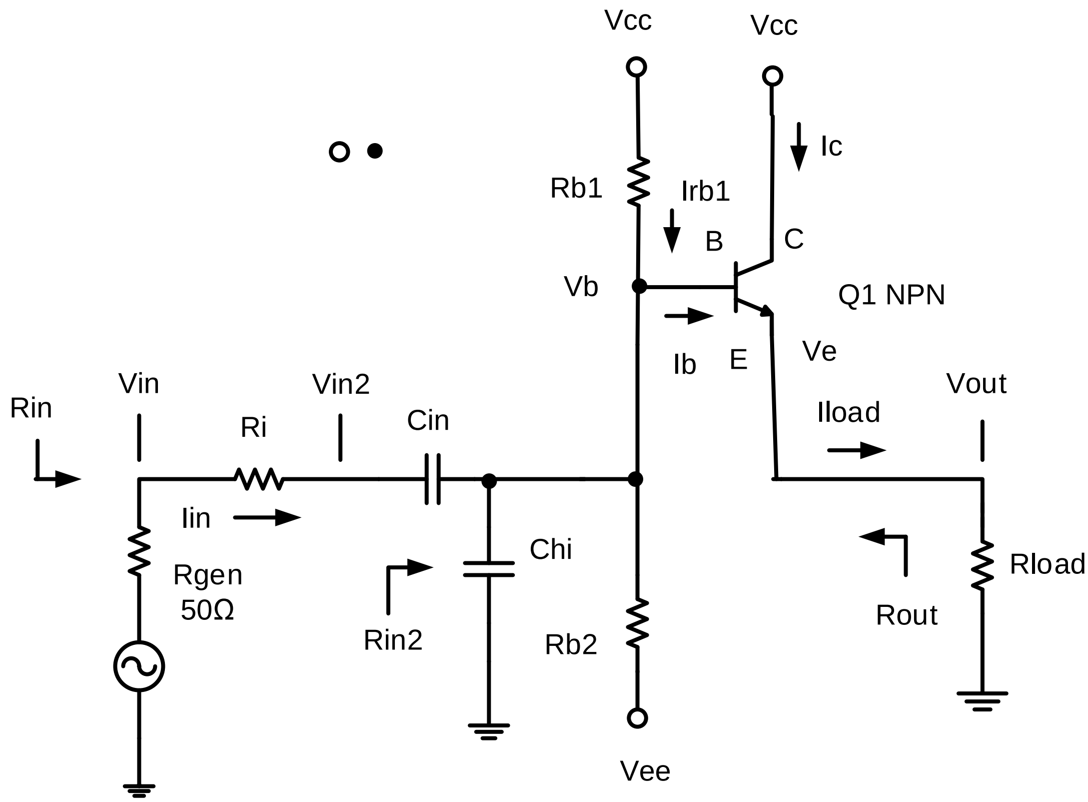

Figure 3 Class B. positive half cycle NPN at peak output voltage.

To start we must find the Vout in peak voltage and Iload as a peak current peak

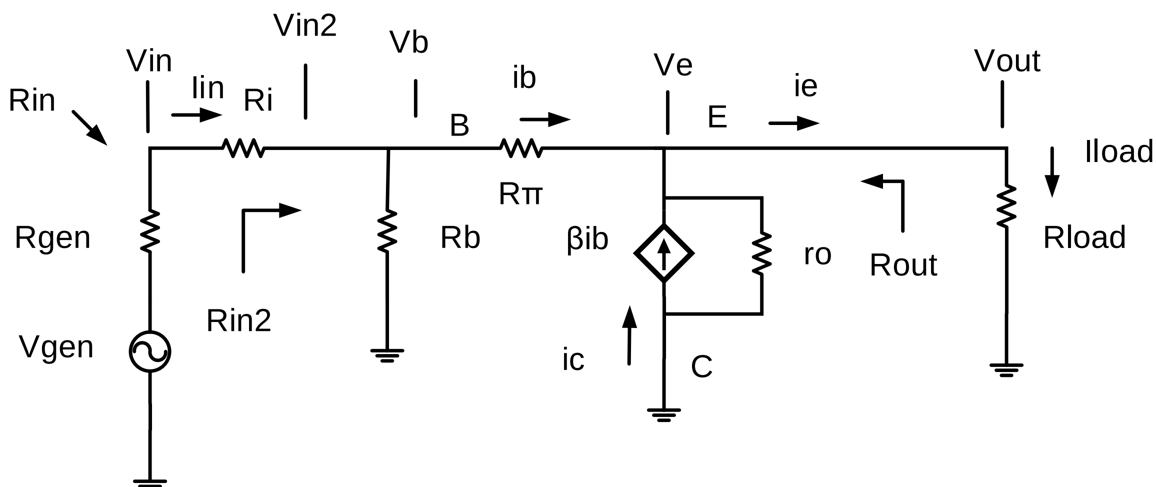

Figure 4 MidBand AC model Class B positive half cycle 2N3904 (NPN) at peak output voltage

Part 2: Class B

Step ClassB 2.1: Find Rb1min, Rb1Max

To find the maximum value for Rb1, Rb2 we will need to calculate the maximum peak base current Ib. Use the minimum β (β_{min} = 100) and maximum i_c peak to give worst case maximum base current.

IloadMax = (Vout $_{peak}$ + 20% Vout $_{peak}$) / Rload **This will include the 20% so we don't design for an edge.**

IeMax = IloadMax all of Ie flows thru the load resistor Rload

Ic = (β / (β +1)) IeMax

IcMax = (βMin / (βMin +1)) IeMax use βMin to maximize Ic.

IbMax = IcMax / βMin Minimum β will give maximum Ib

Step ClassB 2.2: Find rπ minimum

The **minimum value of rπ** is when Ic is maximum and β is minimum.

vt = 26mV

rπMin = (βMin * vt) / IcMax Smallest r_π is when Ic is maximum***.*** Use βMin

rπ = (β * vt) / Ic at the rated Vout not the minimum use βAC from curves. Used for calculating frequency response, input and output impedance.

Step ClassB 2.3: Maximum voltage on the base.

Vb_{max} = Vout +20%Vout + Vbe = VoutMax + Vbe **Vout is the peak value.**

Step ClassB2.4: Maximum value of Rb1.

We need to find the maximum value of Rb1 and Rb2 we must stay below that maximum to insure that there is enough current for the base drive when the output Vout is at maximum

The maximum value Rb1, Rb2 should not be exceeded when selecting a value for Rb1, Rb2.

$Rb1_{max}$ = (Vcc – Vb_{max}) / ib_{max} Positive NPN BJT half.

Set $Rb2_{max}$ = $Rb1_{max}$ **Both are set equal to keep bases balanced and centered between the power supplies.**

Step ClassB 2.5: Find value of Rb1, and Rb2 based on your chosen value of Rin.

When Vin = 0 both of the BJTs are off i.e. high impedance looking into base we see **Rin2 = Rb1 || Rb2**. Rin = Ri + Rb1|| Rb2

Rin2 = Rb1 || Rb2 when **Vin = 0 will not yield the correct value of Rb1, Rb2** because the BJT is off in high impedance state.

We will Calculate **RinW requested where the NPN is on, Vout is maximum positive so we can ignore PNP transistor.**

We are looking for the case where Vin = maximum when Vout = maximum and Rin = requested

Consider only positive half cycle NPN on and PNP off.

Calculate from your chosen RinW

From RinW requested solve for Rin2W requested to meet input requirement.

Rin2W = RinW – Ri requested Rin2.

Step ClassB 2.6: Resistance looking into the base of the transistor

rπ is from step: **ClassB 2.1**

RbaseMin = rπMin + (Rload || ro)(βmin + 1).

Rbase at the Vout required

Rbase = rπ + (Rload || ro)(β + 1). Resistance looking into the base of the transistor at the Vout requirement.

Remember Rb = Rb1 || Rb2 and since Rb1 = Rb2 therefore Rb1 = Rb2 = Rb*2.

Now solve for Rb requited to meet Rin. **Use beta AC not the β_{min} = 100**

Rin2W = RinW – Ri The required resistance a base of the transistor.

Rin2W = Rb || Rbase

Rearrange to solve for Rb.

Therefor **Rb = 1/(1/Rin2W -1/Rbase)**. The Rb required to meet RinW requested.

Now solve for Rb1 and Rb2

Because Rb = Rb1 || Rb2 and Rb1 = Rb2

Therefor Rb1 = Rb2 = 2 * Rb

Check to see if Rb1, Rb2 are below the maximum values for Rb1, Rb2.

Is Rb1 < Rb1Max from **Step ClassB2.4: Maximum value of Rb1.**

Check Rin versus **RinW** The calculated versus the requested value.

Rin2 = (Rb1 || Rb2) || (rπ + (Rload || ro)(β + 1)).

Rin = Rin2 + Ri calculated value.

Part 3 Find Rin, Rout

Step ClassB 3.1:

Use βac not Bmin = 100 from curves to calculate Rin, Rout AC values

Calculations are at the Vout peak values i.e. one transistor on

Step ClassB 3.2: Calculate Rin.

Use the rπ not rπMin from Step ClassB 2.1:

Rin2 = (Rb1 || Rb2) || (rπ + (Rload || ro)(β + 1))

Rin = Ri + Rin2 calculated Rin

Step ClassB3.3: Calculate Rout. Consider only positive half cycle NPN on and PNP off.

Rout = (ro || ((rπ + (Rb1 || Rb2 || (Ri + Rgen))))) / (β +1) Looking into the transistor emitter.

Part 4: Voltage Gain Av, Current gain Ai

Step ClassB 4.1: Av Voltage gain

Vin2 = Vout + Vbe from Vout required.

Rin2 from **Step ClassB 2.6:**

Iin = Vin2 / Rin2

Vbe = 0.7V

Vout = 0 if Vin2 < ± 0.7V

Vout = Vin2 – 0.7V if Vin > 0.7v case of positive Vout required.

Vout = Vin2 + 0.7V if Vin < -0.7v

Vri = Iin * Ri voltage drop across Ri.

Vin = Vin2 + Vri

The Av at maximum Vout AC signal is **Av** = Vout / Vin = (Vin - Iin* Ri - Vbe) / Vin

Vin2 = Vin – Iin* Ri

Av = Vout / Vin = (Vin – Iin * Ri - Vbe) / Vin

Therefor calculate at maximum Vout

Step ClassB 4.3: VgenOC the open circuit Vltage set on the signal source Class B

Vin = Vin2 + Vri   AC signal

VgenOC = Vin + Iin * Rgen   The Open circuit voltage set on the signal source.

Step ClassB 4.4: Ai current gain

Ai = Iload / Iin = (Vout / Rload)/ (Vin / Rin) = Av (Rin / Rload)

Step ClassB 4.5: G, and GdB power gain

G = Av * AI

GdB = 10log(G)

Part 5: Frequency response.

We do not need to the Bandwidth shrinkage factor because we have only 1 break point for each Fl, and Fh.

Step ClassB 5.1: Calculate low frequency cutoff.

FL = 1 / (2π Cin (Rin2 + Ri +Rgen))

Cin = 1/(2π FL (R seen by Cin)).

Step ClassB 5.2: Calculate High frequency cutoff.

FH = 1 / (2π Chi (Rin2 || (Ri +Rgen)))

Chi = 1 / (2π FH (R seen by Chi)).

This section is the design of the Class AB push pull amplifier*.*

Section 2:

Class AB push pull stage.

Part 1 ClassAB: Introduction

The class AB amplifier operates as a class A amplifier when the load current is less the designed quiescent current. In class A operation both the NPN and the PNP BJT are on at Vin =0V Vout = 0v so Iload = 0 therefore all of the bias current (quiescent) flows thru both transistors. The 3 diodes act as constant voltage sources along with the 2 Rb1, Rb2 resistors to supply a voltage on the 2 bases of both transistors to turn the both on. If we did not have the emitter resistors Re1, and Re2 to control the current flow the transistors would over heat. When calculating the loop current for the bias the value of the emitter resisters will set the bias current.

When the input voltage raises and the load current exceeds the quiescent current, the PNP transistor will be off. The power amplifier will be operating as a class B amp and all of the output current flow is from the NPN transistor. When Vin is negative the reverse with be true with NPN off and the PNP sinking all of load current.

The class AB **requires** Rb1 and Rb2 so the push pull stage will be bias properly.

Vcc = - Vee **Need both supplies equal but opposite with a center ground.**
Vin = Vin2 + Iin * Ri.
The input signal voltage calculated from Vout and overall Voltage gain Av
Vin = Vout / Av

Av at Vout max = Vout / Vin

We design the positive half cycle (NPN) and copy to the negative half.

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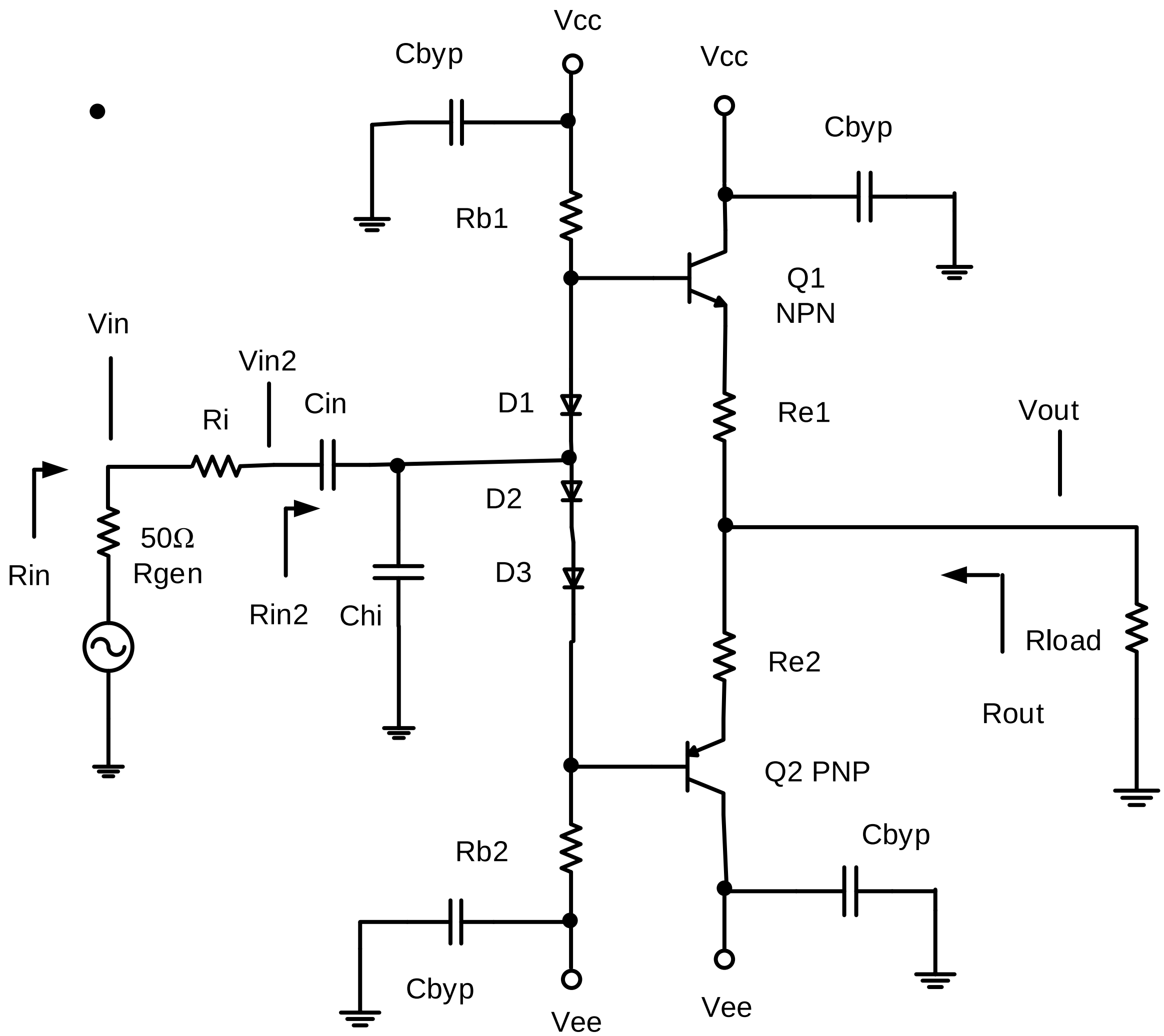
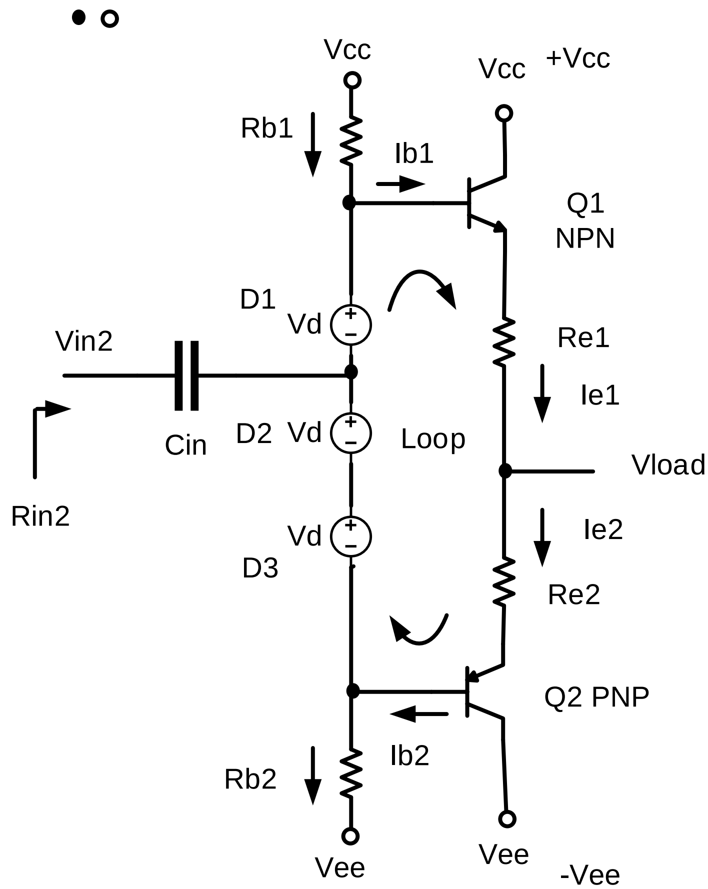


Class AB push pull stage



Bias current (quiescent current) diagram

Part 2 ClassAB: solve bias current a Vin = 0v

Step ClassAB 2.1: write loop equations to solve for bias current.

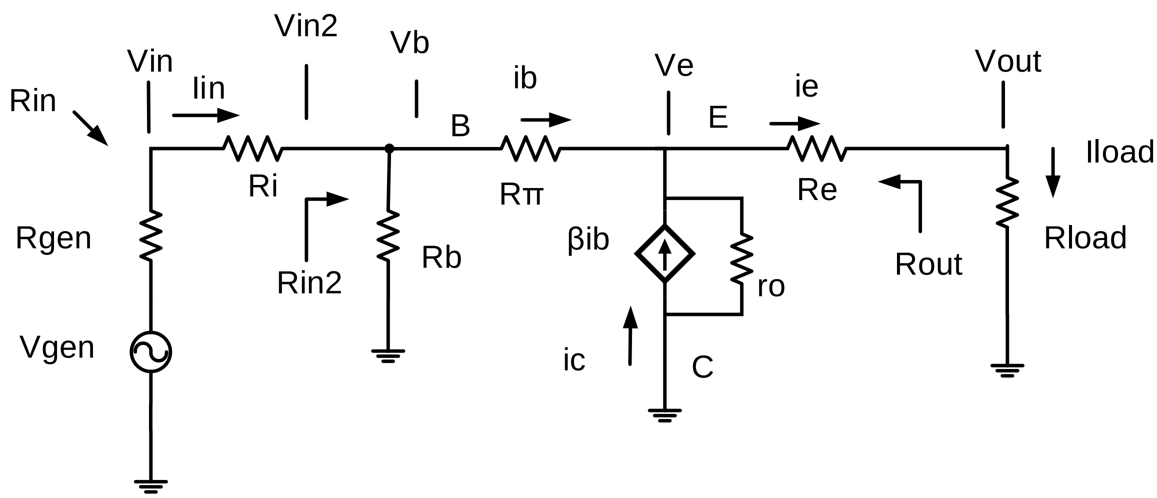
Write the loop equation around the loop to solve for Re1 and, Re2.

Given: I_C = Design bias Ic value when Vin = 0V this is the quiescent current the amplifier in class A range

$I_E = I_C\ (\beta_{min} + 1) / \beta_{Min}$ **Find I_E from the given collect current IcQ.**

Loop equation **0 = -Vd – Vd – Vd + Vbe1 + Ie Re1 + Ie Re2 + Vbe2**

Solve for Re1 + Re2 set Re1 = Re2.



Small signal Class AB positive half cycle 2N3904 (NPN) at peak output voltage

Part 3 ClassAB: find Min and Max Rb1,Rb2.

Step ClassAB 3.1: Find Rb1Max, Rb2Max

We will calculate the maximum peak base current IbMax. Use the minimum β (β_{min} = 100) and maximum i_c peak to give worst case maximum base current IbMax.

IloadMax = (Vout $_{peak}$ + 20% Vout $_{peak}$) / Rload **This will include the 20% so we don't design for an edge.**

IeMax = IloadMax includes 20%

IcMax = (βMin / (βMin +1)) IeMax use βMin to maximize Ic.

IbMax = IcMax / βMin   Use Minimum β to give maximum Ib

Re1 = Re2   from loop equation. See Step ClassAB 2.1

Step ClassAB 3.2: Maximum value of Rb1, and Rb2.

Solve for Rb1Max, and Rb2Max the same as for the class B but **must include Re** in the solution.

Maximum voltage on the base, must include **voltage drop on Re.**

Voltage across Re1 at maximum load current.

VbMax = Vout +20%Vout + Vbe + IeMax * Re1

Rb1Max = (Vcc – VbMax) / ibMax Rb2Max, Rb1Max set equal to each other.

With class AB Rb1, Rb2 cannot exceed Rb1Max, and Rb2Max because there must be enough current to keep the diodes D1, D2, and D3 forward biased so they will act as stable voltage sources. The current Irb1 thru Rb1 must be larger than I_BMax

Step ClassAB 3.2: Minimum r_π

The minimum value of Rπ is when Ic is maximum and β is minimum.

vt = 26mV

$R\pi_{min}$ = (βmin * vt) / IcMax

Rπ = (β * vt) / Ic_Q for Ic_Q = 10ma depends on design requirements of IcQ

Step ClassAB 3.3: Calculate from requested Rin the value of Rb1, and Rb2

Now for the **value of Rb1** we must consider the input impedance requirement.

Where Rin = Ri +Rin2

We are looking for the case where Vin = max, Vout = max, and Rin = requested Rin

Consider only positive half cycle NPN on, and PNP off.

Rb = Rb1 || Rb2 **The value of Rb1, and Rb2 needed to meet the requested Rin**

Remember Rb = Rb1 || Rb2 and Rb1 = Rb2 therefore Rb1 = Rb2 = Rb*2.

RbaseMin = rπMin + (ro || (Rload + Re1)) * (βMin + 1) ***β_{min} = 100 worse case***

Rbase = rπ + (ro || (Rload + Re1)) * (β +1)

Now solve for Rb requited to meet Rin.

Rin2 = Rb || Rbase

Step ClassAB 3.4: The Rb to meet the requested RinW

Where RinW = Ri +Rin2W

Rin2W = RinW – Ri **Rin2 requested**

Rin2W = RbW || Rbase

Therefore, solve for RbW

RbW = 1 / (1/Rin2W -1/Rbase). The RbW requested Rb = Rb1||Rb2.

Rb1 = Rb2 = RbW * 2 Set values of Rb1, and Rb2 from required RbW

Rin2 = (Rb1 || Rb2) || (Rπ + (ro || (Rload + Re1))(β + 1))

Step ClassAB 3.5: Calculate Rin. Check Rin use βac from curves

Use β from curves to calculate Rin, Rout, and Av

Check Rin required. And Rb1, Rb2 are < Rb1Max ,Rb1Max

Rin2 = (Rb1 || Rb2) || (rπ + (ro || (Rload + Re1))(βac + 1))

Rin = Ri + Rin2

Step ClassAB 3.6: Calculate Rout. ClassAB

Consider only positive half cycle NPN on, and PNP off. Calculate at Vout maximum.

BJTemitter =(r_o || ((r_π + Rb1 || Rb2 || (Ri + Rgen)))) / (β +1) ***Looking into the emitter***

Rout = Re1 + BJTemitter

Part 4 Class AB: Voltage gain Av, Ai current gain

Step ClassAB 4.1: Voltage gain Av

Vin = Vin2 (Ri + Rin2) / Rin2	Input signal voltage divider from input to base.
Vout = v_e (Rload / (Re + Rload))	Output voltage divider from emitter to Vout
RloadE = ro || (Re + Rload)	load seen by the emitter

v_e = ib (β +1) (ro ||(Re +Rload)) = ie RloadE **v_e = AC output signal at the emitter use β_{AC}**

Vout = v_e (Rload / (Re + Rload)) = i_b (β + 1) (RloadE) * (Rload / (Re + Rload))

Vin2 = i_b Rπ + i_b (β + 1) (ro || (Re + Rload)) = i_b Rπ + i_b (β + 1) (RloadE)

use this equation to solve for Av2 the voltage gain from the Base to the output across Rload

Av2 = Vout / Vin2 = **(β + 1) (RloadE) * (Rload / (Re + Rload)) / (Rπ + (β + 1) (RloadE)**

Substitute in Av2 to solve Av overall

Av = Vout/ Vin = Av2 * ((Rin2 / (Ri + Rin2))

Input Divider	**Output Divider**	**Gain from base to emitter**

Av = ((Rin2 / (Ri + Rin2)) * (Rload / (Re + Rload)) * ((β + 1) RloadE / (Rπ + (β + 1) (RloadE)

Step ClassAB 4.2: Generator Open circuit voltage ClassAB

Vin = Vin2 + Iin * Ri   AC signal

VgenOC = Vin + Iin * Rgen   The Open circuit voltage set on the signal source.

Step ClassAB 4.3: Current Gain Ai ClassAB

Vin2 = Vout / Av2   voltage gain at base.

Iin = Vin2 / Rin2

Ai = Iload / Iin = (Vout / Rload)/ (Vin / Rin) = Av (Rin / Rload)

Step ClassAB 4.4: Power Gain G Pout / Pin and Power gain in dB GdB

G = Pout / Pin = (Vout * Iload) / (Vin * Iin) = Av * Ai

GdB = 10Log (G)

Part 5: Class AB frequency response.

We do not need to the Bandwidth shrinkage factor because we have only 1 break point for each Fl, and Fh.

Step ClassAB 5.1: Calculate low frequency cutoff. Do not need to use band shrinkage factor because only one capacitor.

FL = 1 / (2π Cin (Rin2 + Ri +Rgen)) at Vout max.

Cin = 1/(2π FL (R seen by Cin)).

Step ClassAB 5.2: Calculate High frequency cutoff. . Do not need to use band shrinkage factor because only one capacitor break point.

FH = 1 / (2π Chi (Rin2 || (Ri +Rgen))) at Vout max.

Chi = 1/(2π FH (R seen by Chi)).