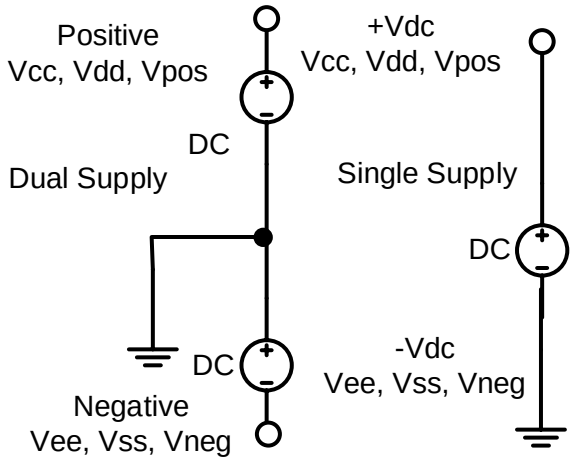
**Common Drain (CD) Design**

Designing procedure of common drain MOSFET amplifier can be grouped into three systematic stages. First, we have to set the Q-point, which is the DC operating point. Since, no specification regarding the Q-point is mentioned in the design requirements. It leaves the designer enough freedom to choose the operating point as necessary for the application. However, it is to remember that the specifications given in terms of input and output impedance, gain, frequency response characteristics and peak output voltages are tight and ultimately restricts the Q-point in a narrow window. It is difficult to analytically derive this point without some intelligent guess and the following steps would work out for the given conditions.




For common drain configuration, the circuit diagram in CD Fig.1. The small signal equivalent model in CD Fig.3.

For this configuration, same steps are involved for the calculation of Rg1, Rg2 and Rs with few minor changes. Note that Rd is absent in this case and we have added an isolation resister Riso because of the capacitive loading of Chi2.

**CD Part 1: Measure the device parameters**

**We need to estimate a Q-point to find an estimate for Vds(sat), ro and gm.**

For the design of the amplifier, the 3 parameter values required are $r_o$ and gm. Derived from the transistor characteristics curve shown in CD Fig.2, one can set an approximate Q-point ($V_{DS}$ and $I_D$) in the active region and measure ro and gm. We will solve for $V_{DS}$ and estimate $I_D$.

**Step CD 1.1**: Estimate the $I_D$ collector current Q-point

For an estimated $I_D$ Q-point use $\mathbf{I_D \approx 2.7^* I_{load}}$ this is not the solution to your design Q-point. We can use an estimated $I_D$ because ro and gm will not very much with small changes in Q-point.

**Step CD 1.2:** The saturated $V_{DS}$ voltage $V_{DS\text{-}sat}$: From the curves CD Fig. 2 estimate $V_{DS}$ (sat) the point where the curve begins to flattens out ≈ 1.0 Vdc

**Step CD 1.3:** Calculate the midpoint $V_S$ and $V_{DS}$ : **Step CD 2.1**

We will start with $V_S$(max) and $V_S$(min).

VoutSource = Vout + $I_{Load}$ * Riso  AC signal Vout at the source terminal.

$V_S$(max) = Vdd – $V_{DS}$sat – (VoutSource + 20%VoutSource)

$V_S$(min) = Vss + VoutSource + 20% VoutSource

$V_S$ = ($V_S$(max) + $V_S$(min)) / 2  Midpoint $V_S$ Q-point

$V_{DS}$ = $V_D$ – $V_S$

**Step CD 1.4:** Find ro, gm, and Vgs.

Plot the estimated Q-point ($V_{DS}$,$I_D$) on the MOSFET characteristics curve.

ro = $\Delta V_{DS}$ / $\Delta I_D$  the slope of a line thru the estimated Q-point

gm = $\Delta I_D$ / $\Delta V_{GS}$  measured around the estimated Q-point this is the gain of the transistor.

Vgs = the Vgs cure closet to your estimated Q-point

**CD Part 2: Find the Q-point start here if given Vds, Id, Vds(sat), ro, and gm.**

**CD Step 2.1: Derive Vs Q- point**

We will start with $V_S$(max) and $V_S$(min).

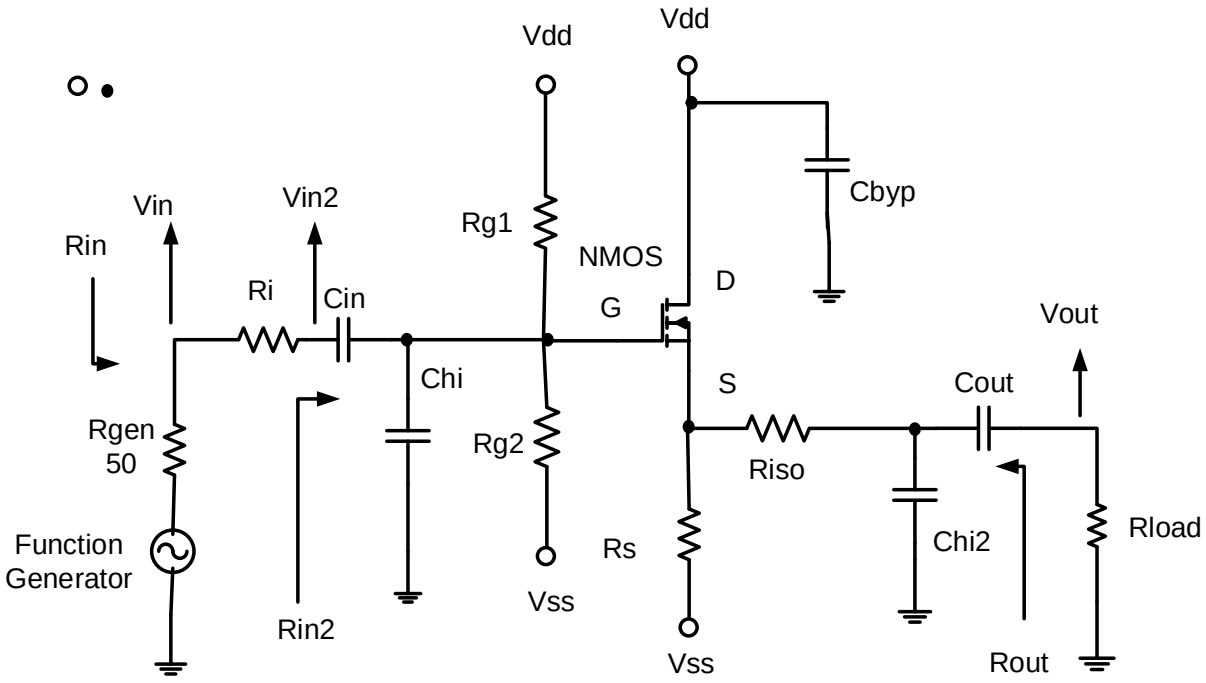
VoutSource = Vout + $I_{Load}$ * Riso  Vout at the source

$V_S$(max) = Vdd – $V_{DS}$sat – (VoutSource + 20%VoutSource)

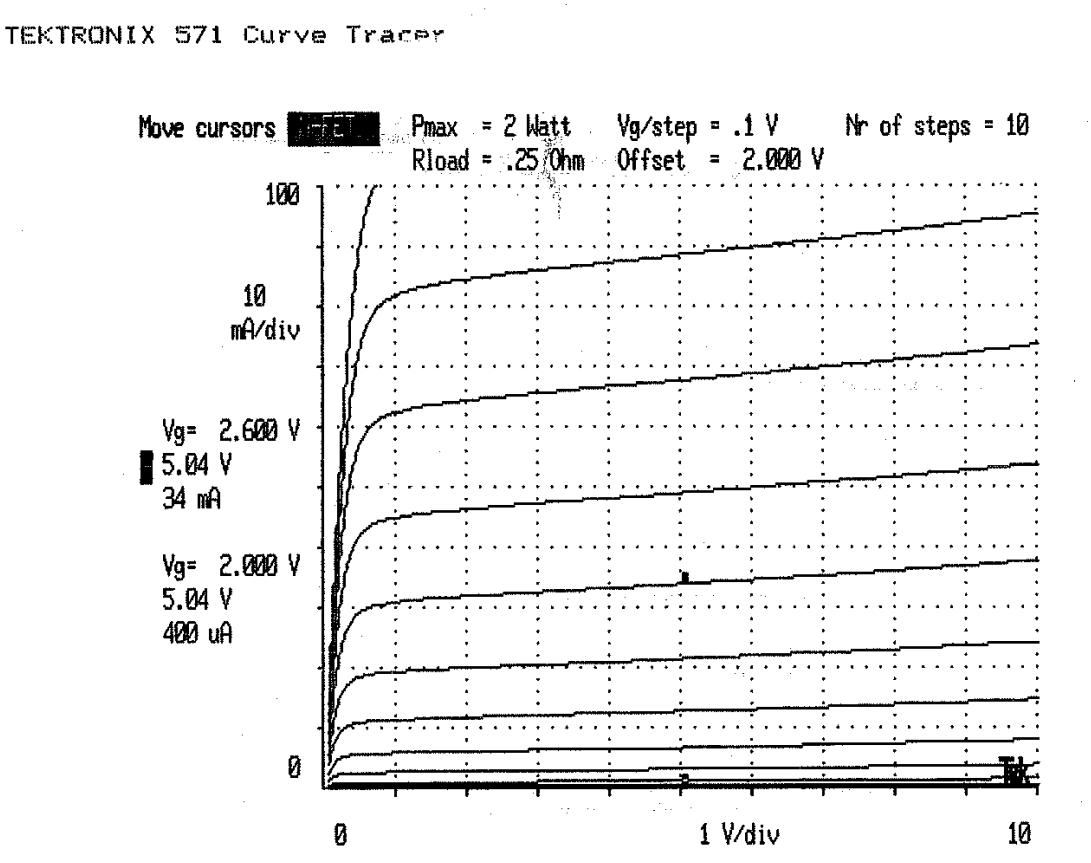
$V_S$(min) = Vss + VoutSource + 20% VoutSource

$V_S$ = ($V_S$(max) + $V_S$(min)) / 2  Midpoint $V_S$ Q-point

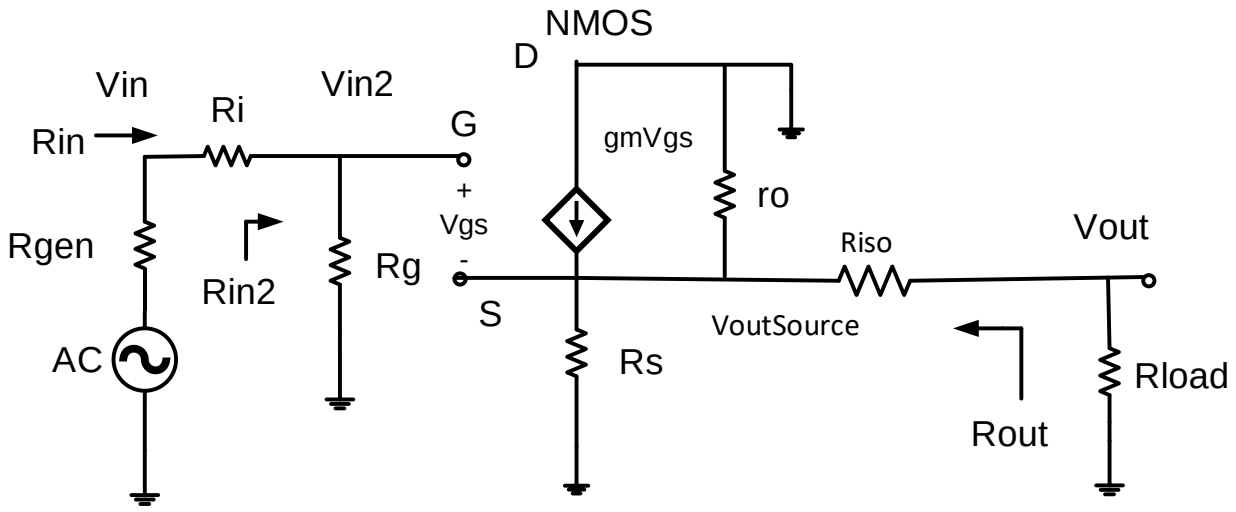
$V_{DS}$ = $V_D$ – $V_S$




CD Figure 1: MOSFET Common Drain CD configuration



CD Figure 2: CD MOSFET curve.




CD Figure 3: Small signal equivalent model for common drain model

**CD Part 3: Determine bias resistors**

**CD Step 3.1: Now find the value of Rs and $I_S$**

We need a higher VoutSource then Vout because of voltage divider Riso, Rload.

**VoutSource = Vout * ( Rload + Riso) / Rload = Vout + ILoad * Riso**

The DC equation: $V_{Rs} = (V_S - Vss) = Rs\, I_S$ Voltage across Rs

The AC equation: $VoutSource = i_s$ ( Rs || ro ||( Rload + Riso) )

Combined equation: $VoutSource = V_{Rs}$ (ro || (Rload + Riso)) / (Rs + (ro || (Rload + Riso)))

$$Rs = \frac{V_{RS}}{V_{out}Source + 20\% V_{out}\,Source} (ro \parallel (Rload + Riso)) - (ro \parallel (Rload + Riso))$$ Rearrange combined equation

Calculate Is

$I_S = I_D = V_{RS} / Rs = (Vs - Vss) / Rs$

Check the power ($I_S$^2 Rs) in the Rs if it is greater than **250mW** to use two source resistors to equal your design value (Rs) ether in series or parallel.

**CD Step 3.2: Calculate Rg1, Rg2. Set Rin to desired value**

$V_G = V_S + V_{SG}$

Rin desired = RinW

Rin2W = RinW – Ri

Rg1 = (Vdd – Vss)/ ($V_G$ - Vss) Rin2W

Rg2 = Rg1 (Vg – Vss) / (Vdd – Vg)

Check Rin meets requirements

Rin2 = Rg = Rg1 || Rg2

Rin = Ri + Rin2

**CD Part 4: Calculate Rin, Rout, Av, and Ai**

**CD Step 4.1: Input Impedance:**

Rin2 = Rg = Rg1 || Rg2
Rin = Rin2 + Ri

**CD Step 4.2: Output Impedance**

Rout = ( Rs || ro || (1 / gm ) )+ Riso

**CD Step 4.3: Calculation of Av Voltage Gain**

Referring to CD Fig.3, let us find $\frac{v_{out}}{v_{in}}$ which would be a key step in calculating Av.

Rin = Ri + Rin2

Rin2 = Rg = Rg1 || Rg2

Rout = (Rs || ro || (1 / gm ) ) + Riso  Looking into the CD amp output.

VoutSource = gm Vsg (Rs || ro || (Rload + Riso))  Voltage across Rload + Riso.

Vout = VoutSource * (Rload / (Rload + Riso))  Voltage divider to Vout from VoutSource.

Voltage at the function generator  Vin = Vin2 (Rin / Rin2)

Voltage at the Gate  Vin2 = Vgs + VoutSource  AC equation.

Vin2 = Vgs + gm Vgs (Rs || ro || (Rload + Riso)) = Vgs ( 1 +gm(Rs || ro || (Rload + Riso)) )

Av3 =  VoutSource / Vin2= gm (Rs || ro || (Rload+ Riso)) / (1 +gm(Rs || ro || (Rload+ Riso))

Av = Vout / Vin =  (Rin2 / Rin) * (Rload / (Rload +Riso) ) * Av3

Thus, the voltage gain should be close to 1. Hence, the output follows the input. So, the Common Drain configuration also known as Source follower.

**CD Step 4.4: Current Gain**

$$\text{Ai} = \frac{Iload}{Iin} = \frac{Vout/_{Rload}}{Vin/_{Rin}} = \text{Av}\frac{\text{Rin}}{\text{Rload}}$$

**CD Step 4.5: Power gain**

G = Pout / Pin = Vout * Iload / Vin * Iin = Av * Ai

In decibels $G_{dB}$ = 10log ( Av * Ai )

**CD Step 4.6: Vin and Voc of Vgen**

Input signal level needed to produce the required output voltage.

Vin = Vout / Av

The open circuit voltage of the generator to produce the required output voltage.

Because of Voltage divider because the output impedance of the Rgen = 50Ω

Vgen = Vin (Rgen + Rin) / Rin

Use this value in LTspice and the laboratory Function generator

**CD Part 5: Frequency response.**

The capacitor values can be calculated as before, the only difference being *n* = 2 for low pass calculations since we are using two capacitors instead of 3.
With the Q-point set after the sequence of steps, we can go for the selection of capacitors and finally connect the signal generator at input and measure the output waveform.

First we will select $C_{in}$, and $C_{out}$ which jointly would set the roll-off beyond the lower cut-off frequency. Set any frequency within the range as your lower cut-off frequency and let us call it $f_L$. Two capacitors will introduce 2 zeros in the transfer function of the system. Because we will set 2 zeros at the same frequency we must use the Band Width Shrinkage factor.

$$\text{BWshrinkage} = \sqrt{2^{\frac{1}{n}} - 1} \quad n = 2$$

Where n is the number of zeros for low frequency breakpoints at same frequency.

Setting 2 frequencies equal, we get,

$f_{Cin} = f_{Cout} = f_L \sqrt{2^{1/2} - 1} = FL * BWshrinage$

Find the C for each breakpoint $f_{Cin}$ , and $f_{Cout}$ , where n = 2.

$$C = \frac{1}{2\pi f_C \, (\text{R seen by C})}$$

Where C is the capacitor that sets the breakpoint $f_C$

R is the Thevenin equivalent resistance seen by the capacitor.

The following table enlists the particular expressions.

| | |
|---|---|
| Rsig | Rgen+Ri |
| $C_{in}$ | Rsig + Rin2 |
| Cout | $R_{Load}$ + Rout |
| $C_{hi}$ | Rsig \|\| Rin2 |
| Chi2 | Rout \|\| Rload |

CD Table 1: Resistance Seen By Capacitors

Chi, and Chi2 on the contrary, sets the high cut-off frequency $f_H$ which is to be set from the specified range.

In this case because Chi, and Ch2 are to the same break point. We must use the band shrinkage factor with n = 2. We need only to find a two poles at $F_h$ / bandshrinage = $f_{chi} = f_{ch2}$ to set the high frequency cutoff.

Set Fchi = Fchi2 = Fh / $\sqrt{2^{1/2} - 1}$ = FH / BWshrinkage

Rin2 = Rg1 || Rg2

R seen by $C_{hi}$ $R_{Chi}$ = (Rgen + Ri) || Rin2

$$C_{hi} = \frac{1}{2\pi f_{Chi} \, (\text{R seen by } C_{hi})}$$

R seen by $C_{hi2}$ $R_{Chi2}$ = Rout || Rload

$$C_{hi2} = \frac{1}{2\pi f_{Chi2}\,(\text{R seen by } C_{hi2})}$$