ECE 3274 MOSFET amplifier design. Richard Cooper

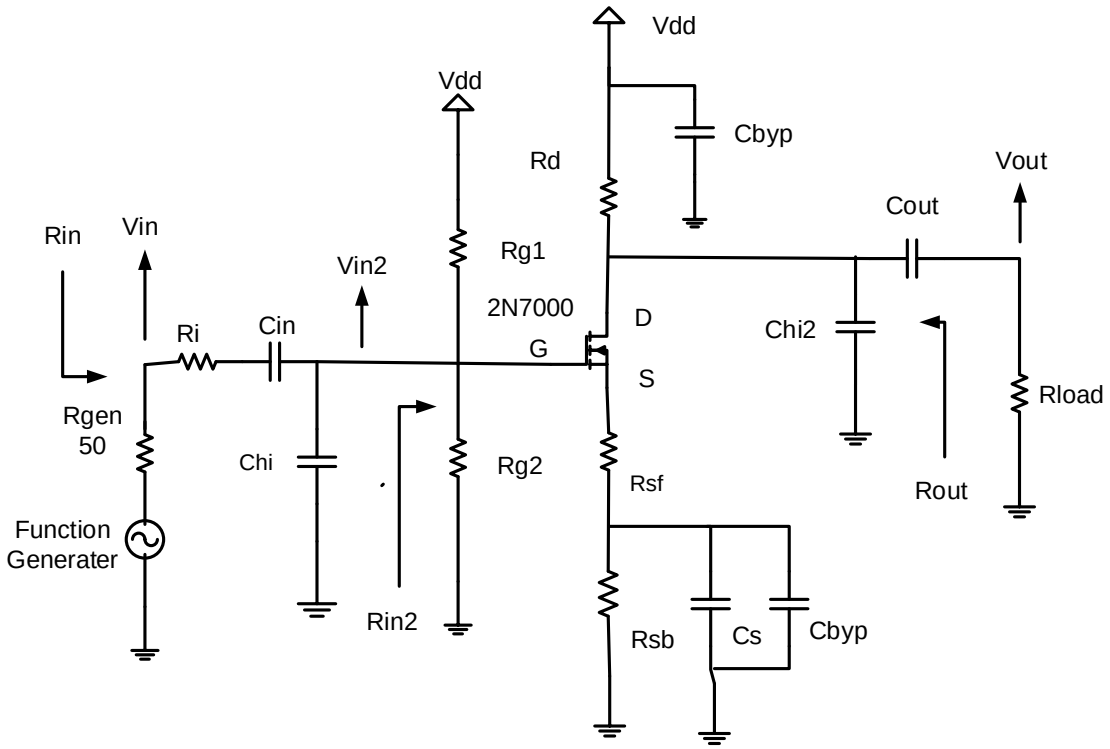
Common Source with source degeneration (partial Rs bypassed)

Common source with source degeneration (CSwRsf)

Designing procedure of common source MOSFET amplifier with source degeneration can be grouped into three systematic stages. First, we have to set the Q-point, which is the DC operating point. Since, no specification regarding the Q-point is mentioned in the design requirements, it leaves the designer enough freedom to choose the operating point as necessary for the application. However, it is to remember that the specifications given in terms of input and output impedance, gain, frequency response characteristics and peak output voltages are fairly tight and ultimately restricts the Q-point in a narrow window. It is difficult to analytically derive this point without some intelligent guess and the following steps would work out for the given conditions.

Common Source with Source Resistance partially Bypassed (CSwRsf)

In this configuration, R_S is bypassed with Cs. The circuit diagram with necessary variables is provided in CSwRsf Fig.1.



CSwRsf Figure 1: MOSFET Common Source

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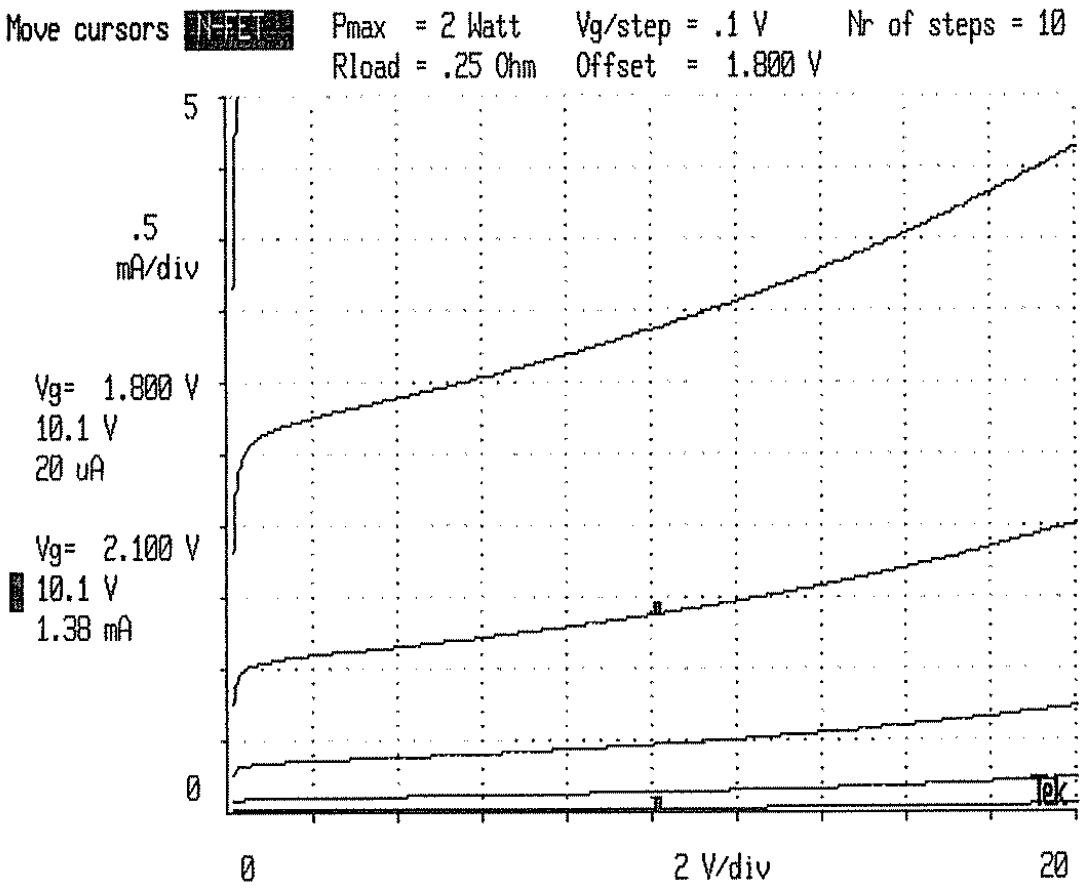
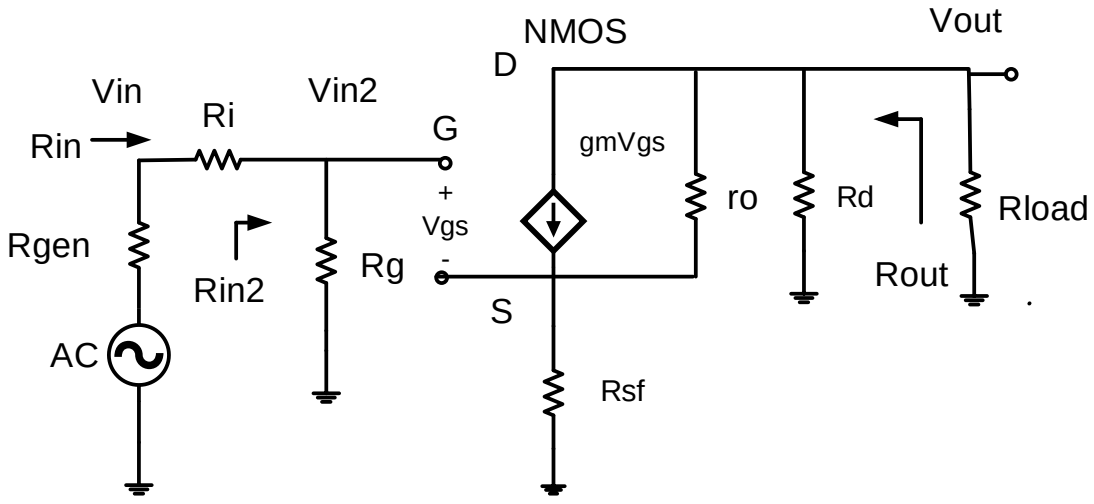


CSwRsf Figure 2: MOSFET characteristics, Example not your Q-point



CSwRsf Figure 3: Common Source Small Signal Equivalent Circuit

CSwRsf Part 1: Measure the device parameters

For the design of the amplifier, the 3 parameter values required are r_o and gm. Derived from the transistor characteristics curve shown in CS Fig.2, one can set an approximate Q-point (V_{DS} and I_D) in the active region and measure ro and gm. We will solve for V_{DS} and estimate ID.

Solve for V_{DS} based on the Vout see below. **Step CSwRsf 1.4**

For an approximate I_D Q-point use $I_D \approx 3.0 * I_{load}$ this is not the solution to your design Q-point. We can use an approximate I_D because ro and gm will not very much with small changes in Q-point.

ro = $\Delta V_{DS} / \Delta I_D$ the slope of a line thru Q-point

gm = $\Delta I_D / \Delta V_{GS}$ measured around Q-point

Plot the estimated Q-point (V_{DS},I_D) on the MOSFET characteristics curve.
From the curves estimate V_{DS}sat the point where the curve begins to flattens out ≈ 1 Vdc

For the design of the amplifier, the 4 parameter values required are Vce_{SAT}, r_o , r_π and β. Derived from the transistor characteristics curve shown in MOSFET above, one can set an approximate Q-point (V_{DS} and I_S) in the active region and measure ro and gm. We will solve for V_{ce} and estimate I_C.

Step CSwRsf 1.1: Choose V_{Rs} Same as Step CSwRef 2.1

V_{Rs} is the voltage across the source resister Rs = Rsf + Rsb

Because V_{GS} will decrease ≈ 2.5mV / ˚ C rise we set V_{Rs}= between 2V to 3V. V_S and Rs will provide negative feedback to stabilize gm and V_{GS}.

Vs = V_{Rs} + Vss Voltage on the MOSFET source terminal.

Step CSwRsf 1.2: Choose I_S estimate.

For an approximate I_S Q-point use $I_S \approx 3.0 * I_{load}$ peak this is not the solution to your design I_S Q-point. We can use an approximate I_S because ro and gm will not change very much with small changes in Q-point.

Step CSwRsf 1.3: V_{DS}sat (V_{DS} saturation voltage)

The V_{DS}sat (V_{DS} saturation voltage) are found from the MOSFET characteristics curve where the curve begins to flatten out ≈ 1 Vdc.

Step CSwRsf 1.4: Calculate the midpoint V_D

Same as **Step CSwRsf 2.2**

Rs partially bypassed Rs = Rsb + Rsf

Midpoint selection will allow for maximum output voltage swing.

We will add 20% to Vout so the design is not on the edge of the solution. This will also help with the additional loading because of high frequency capacitors as the frequency approaches the high frequency break points.

$V_{D(max)} = V_{DD}$ - (Vout + 20%Vout)

$V_{D(min)} = V_S + V_{DS}$sat + (Vout + 20%Vout)

$V_D = (V_{D(max)} + V_{D(min)}) / 2$ Midpoint V_D Q-point

$V_{DS} = V_D – V_S$ This is the Q-point V_{CE}

Step CSwRsf 1.5 find ro, gm, Vsd_{SAT}.

ro = $\Delta V_{DS} / \Delta I_C$ the slope of a line thru Q-point drain to source resistance of Hybrid Pie model.

gm = $\Delta I_D / \Delta V_{GS}$ measured around Q-point est.

Vds_{SAT} = the V_{DS} where the VI curve begins to flatten. V_{DS}sat ≈ 1V.

Plot the estimated Q-point (V_{DS},I_D) on the MOSFET characteristics curve.

CSwRsf Part 2: Determine the Q-point.

Start with your MOSFET determine the Q-pint and select the bias 4 resistors.

CSwRsf Step 2.1: Choose V_{Rs}

V_{Rs} is the voltage across the source resister Rs = Rsf + Rsb

Because V_{GS} will decrease ≈ 2.5mV / ˚ C rise we set V_{Rs}= between 2V to 3V. V_S and Rs will provide negative feedback to stabilize gm and V_{GS}.

Vs = V_{Rs} + Vss Voltage on the MOSFET source terminal.

CSwRsf Step 2.2: Calculate the midpoint V_D.

Midpoint selection will allow for maximum output voltage swing.
We will add 20% to Vout so the design is not on the edge of the solution.

$V_{D(max)} = V_{DD}$ - (Vout + 20%Vout)
$V_{D(min)} = V_S + V_{DS}$ sat + (Vout + 20%Vout)
$V_D = (V_{D(max)} + V_{D(min)}) / 2$ Midpoint V_D Q-point
$V_{DS} = V_D - V_S$

CSwRsf Step 2.3: Calculate R_D.
The DC equation: $V_{RD} = V_{DD} - V_D = Rd\, I_D$ Voltage across Rd
The AC equation: $Vout = i_d (Rd \parallel ro \parallel R_L)$
Combined equation: $Vout = V_{RD} (ro \parallel R_L) / (Rd + (ro \parallel R_L))$
Rewriting to solve for Rd.

$$Rd = \frac{V_{DD} - V_D}{V_{out} + 20\%V_{out}} (ro \parallel R_L) - (ro \parallel R_L)$$

CSwRsf Step 2.4: Calculate I_D.
$I_D = (V_{DD} - V_D) / Rd$
$I_S = I_D$
Thus, Q-point is (V_{DS}, I_D).

CSwRsf Step 2.5: Find DC bias V_{SG}, and V_G
Plot the Q-point (V_{DS}, I_D) on the MOSFET characteristics curve.
From the curves, find V_{GS}.
$V_G = V_S + V_{GS}$

CSwRsf Part 3: Determine bias resistors.

CSwRsf Step 3.1: Calculate R_{g1}, R_{g2}. Based on required value for Rin.
Set Rin to desired value

$V_G = V_S + V_{GS}$ DC bias point values.
Rin desired = RinW The desired RinW = Rin
Rin2W = RinW – Ri The desired Rin2W = Rin2
Rg1 = ((Vdd – Vss) / (V_G - Vss)) * Rin2W
Rg2 = Rg1 (V_G – Vss) / (Vdd – V_G) Voltage across Rg2 divided by the current thru it (same as thru Rg1)

Check Rin meets requirements
Rin2 = Rg = Rg1 || Rg2

Rin = Ri + Rin2 Check to see if meets Rin desired.

CSwRsf Step 3.2: Calculate Rsf from required gain.
Recall:
$I_S = I_D$
Rs = V_{Rs} / I_S = **Rsf + Rsb** total DC source resister.

Derive equation for calculating Rsf from desired Av.
Recall Rin2 = Rg = Rg1 || Rg2

Vout = - gm Vgs(Rd || Rload || (r_o + Rsf || 1/gm)

Vin = ((Rin2 + Ri) / Rin2) Vin2

Vin2 = Vgs + v_s AC voltage signal at Vin2.

Vin2 = Vgs + (gm Vgs) * Rsf = Vgs (1 +gm Rsf)

Voltage gain from Vin2 to Vout Av2

Av2 = Vout / Vin2 = (- gm Vgs(Rd || (r_o + (Rsf || 1/gm)) || Rload)) / Vgs (1 +gm Rsf)
Voltage gain at Vin2 Av2

Cancel out Vgs
Av2 = (- gm (Rd || (r_o + (Rsf || 1/gm)) || Rload)) / (1 +gm Rsf)

Av = (Rin2 / (Rin2 +Ri))* Av2 Av it terms of Av2

Av = Vout / Vin = (Rin2 / (Rin2 + Ri)) * (- gm(Rd || (r_o +(Rsf || 1/gm)) || Rload) / (1 +gm Rsf))

Solve for Rsf.

Rearrange Av = - gm (Rin2/(Rin2 + Ri)) * (Rd || Rload || (r_o + (Rsf || 1/gm)) / (1 + gm Rsf)

1 +gm Rsf = - gm (Rin2/(Rin2 + Ri)) * (Rd || Rload || (r_o + (Rsf || 1/gm))) / Av

Note: Av is negative.

Rsf = - ((Rin2/(Rin2 +Ri)) * (Rd || Rload || (**ro + (Rsf || 1/gm**))) / Av)) - 1 / gm

We do not have Rsf yet so we will approximate the term

ro + Rsf || 1/gm ≈ ro

Yielding:

Note: Av is the desired Voltage gain

Rsf = - (((Rin2/(Rin2 + Ri)) * (Rd || Rload || ro)) / **Av**) - 1/gm

Rsb = Rs - Rsf

CSwRsf Step 3.2: Calculate R_{g1}, R_{g2}. Based on required value for Rin.
Set Rin to desired value

$V_G = V_S + V_{SG}$ DC bias point values.
Rin desired = RinW
Rin2W = RinW – Ri desired Rin2W
Rg1 = ((Vdd –Vss) / (V_G - Vss)) * Rin2W
Rg2 = Rg1 (V_G – Vss)/ (Vdd – V_G)

Check Rin meets requierments
Rin2 = Rg = Rg1 || Rg2

Rin = Ri + Rin2

CSwRsf Part 4: Calculating impedance and Gain

Refer to the small signal equivalent of the circuit you have just built in CS Fig. 3. We can calculate the following:

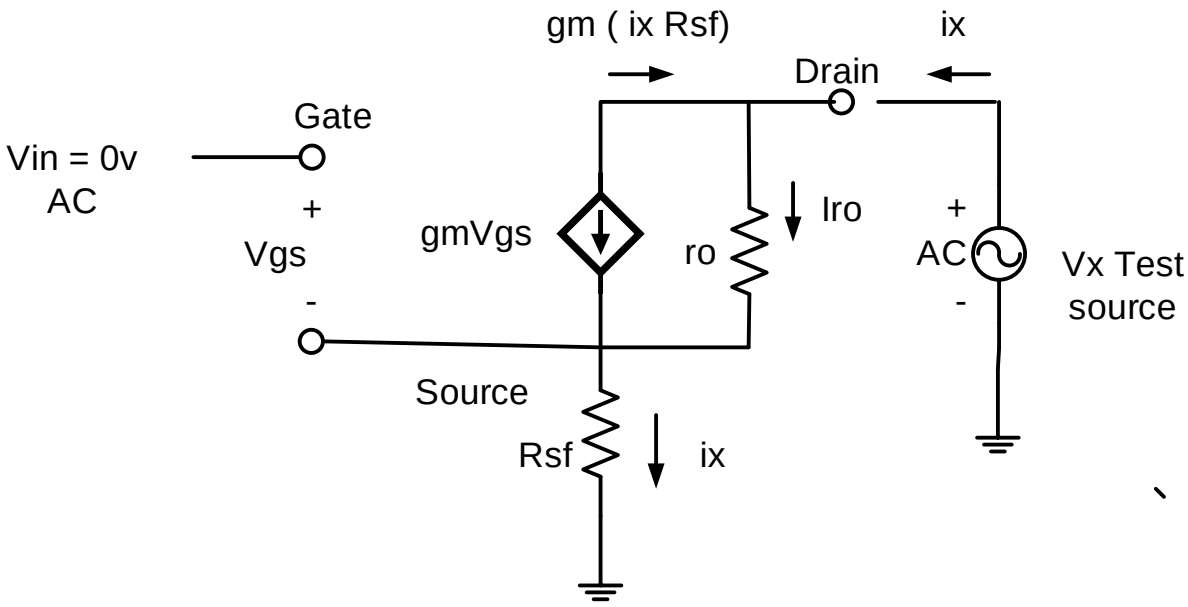
CSwRsf Step 4.1: Input Impedance:

Rin2 = Rg = Rg1 || Rg2
Rin = Rin2 + Ri

CSwRsf Step 4.2: Output Impedance Rout.

Derivation of the equation for the resistance looking into the drain.

I_x current from the test voltage v_x applied to the Drain of MOSFET we will ignore Rd for now.



CSwRfs Figure 4: Small signal equivalent circuit Drain resistance.

Derive the equation for the resistance looking into MOSFET Drain.

Apply an AC test voltage Vx to the drain and measure the current i_x.

Vgs = - i_x Rsf Vgs caused by applied test voltage, v_g gate voltage = 0v (AC signal voltage).

- gm(- i_x Rsf) Current in the dependent source of MOSFET (AC signal current)

Current flowing thru r_o $i_{ro} = i_x$ - gm(- i_x Rsf) = i_x + gm i_x Rsf

$V_x = r_o (i_x + gm\ i_x\ Rsf\ ) + i_x\ Rsf$ divide thru by i_x

The equation for the **resistance looking into MOSFET Drain**.

R looking into drain $\mathbf{V_x / i_x} = ro\ (1 + gm\ Rsf) + Rsf = ro + ro\ gm\ Rsf + Rsf$

Now apply Rd in parallel with impedance looking into MOSFET Drain.

Rout = Rd || (ro (1 + gm Rsf) + Rsf) = Rd || (ro + ro gm Rsf + Rsf)

CSwRsf Step 4.3: Voltage Gain calculated
Derive the Av equation.

Recall Rin2 = Rg = Rg1 || Rg2
Vout = - gm Vgs (AC load) = - gm Vgs(R_D || Rload || (ro + ro gm Rsf + Rsf))
Vin = (Rin2 + Ri / Rin2) Vin2
Vin2 = Vout / Av2
Vin2 = Vgs + v_s AC voltage signals.

i_s = gm * Vgs AC signal current not bias current Is

Vin2 = Vgs + Rsf * i_s = Vgs + Rsf(gm * Vgs) = Vgs (1 +gm Rsf)

Av2 = Vout / Vin2 = = - gm Vgs(R_D || Rload || (ro + ro gm Rsf + Rsf)) / Vgs (1 +gm Rsf)

Av = Vout / Vin = - ((Rin2/(Rin2 + Ri)) * gm Vgs(Rd || Rload || (ro + ro gm Rsf + Rsf)) / Vgs (1 +gm Rsf)

Rearrange Av = - gm((Rin2/(Rin2 + Ri)) (Rd || Rload || (ro + ro gm Rsf + Rsf)) / (1+ gm Rsf)

This is the calculated value for Av using the components that we selected.

Av = Vout / Vin = - gm ((Rin2/(Rin2 + Ri)) (Rd || Rload || (ro + ro gm Rsf + Rsf)) / (1+ gm Rsf)

This gain will be higher than out design value because we made an approximation in step CSwRsf Step 3.2 above for finding Rsf **ro + Rsf || 1/gm ≈ ro.**

CSwRsf Step 4.4: Current Gain

$$\mathrm{Ai} = \frac{Iload}{Iin} = \frac{Vout/_{Rload}}{Vin/_{Rin}} = \mathrm{Av}\frac{\mathrm{Rin}}{\mathrm{Rload}}$$

CSwRsf Step 4.5: Power gain
G = Pout / Pin = Vout * Iload / Vin * Iin = Av * Ai
In decibels G_{dB} = 10log (Av * Ai)

CSwRsf Step 4.6: Vin and Voc of Vgen
Input signal level need to produce the required output voltage.
Vin = Vout / Av

The open circuit voltage of the generator to produce the required output voltage.
Because of Voltage divider because the output impedance of the Rgen = 50Ω

Vgen = Vin (Rgen + Rin) / Rin Set this value in function generator.

Use this value in LTspice and the laboratory Function generator

CSwRsf Part 5: Frequency response

With the Q-point being set after the sequence of steps, we can go for the selection of capacitors and finally connect the signal generator at input and measure the output waveform.

First we will select C_{in}, C_{out} and C_S which jointly would set the low cut-off frequency. Set any frequency within the range as your lower cut-off frequency and let us call it f_L. Three capacitors will introduce 3 zeros in the transfer function of the system. Because we will set 3 zeros at the same frequency we must use the Band Width Shrinkage factor.

$$\text{BWshrinkage} = \sqrt{2^{\frac{1}{n}} - 1}$$

Where n is the number of poles for low frequency breakpoints at same frequency.

$$f_L = \frac{f_{C_{in}} + f_{C_{out}} + f_{C_E}}{3\sqrt{2^{\frac{1}{3}} - 1}}$$

Setting 3 frequencies equal, we get,

$f_{Cin} = f_{Cout} = f_{CS} = f_L \sqrt{2^{1/3} - 1}$ = FL * BWshrinkage

Find the C for each breakpoint f_{Cin} , f_{Cout} , and f_{CE} where n = 3.

$$\text{C} = \frac{1}{2\pi f_C \,(\text{R seen by C})}$$

Where C is the capacitor that sets the breakpoint f_C

R is the Thevenin equivalent resistance seen by the capacitor.

R_{Cs} = Rsb || (Rsf + (ro + Rd || R_{Load}) || (1 / gm))

The following table enlists the particular expressions.

Rsig	Rgen+Ri
C_{in}	Rsig + Rin2
Cout	RL + Rout
C_S	Rsb || (Rsf + (ro + (Rd || R_{Load})) || (1 / gm))
C_{hi}	Rsig || Rin2
C_{hi2}	Rout || Rload

CSav Table 1: Resistance Seen By Capacitors

C_{hi}, on the contrary, sets the higher cut-off frequency f_H which is to be set from the specified range.

In this case because Chi, and Ch2 are to the same break point. We must use the band shrinkage factor with n = 2. We need only to find a two poles at F_h / band shrinkage = $f_{chi} = f_{ch2}$ to set the high frequency cutoff.

Set Fchi = Fchi2 = Fh / $\sqrt{2^{1/2} - 1}$ = FH / BWshrinkage

Rin2 = Rg1 || Rg2

R seen by C_{hi} R_{Chi} = (Rgen + Ri) || Rin2

$$C_{hi} = \frac{1}{2\pi f_{Chi}\,(\text{R seen by } C_{hi})}$$

R seen by C_{hi2} R_{Chi2} = Rout || Rload

$$C_{hi2} = \frac{1}{2\pi f_{Chi2}\,(\text{R seen by } C_{hi2})}$$