Design tools for Two stage DC coupled CS – CC amplifier

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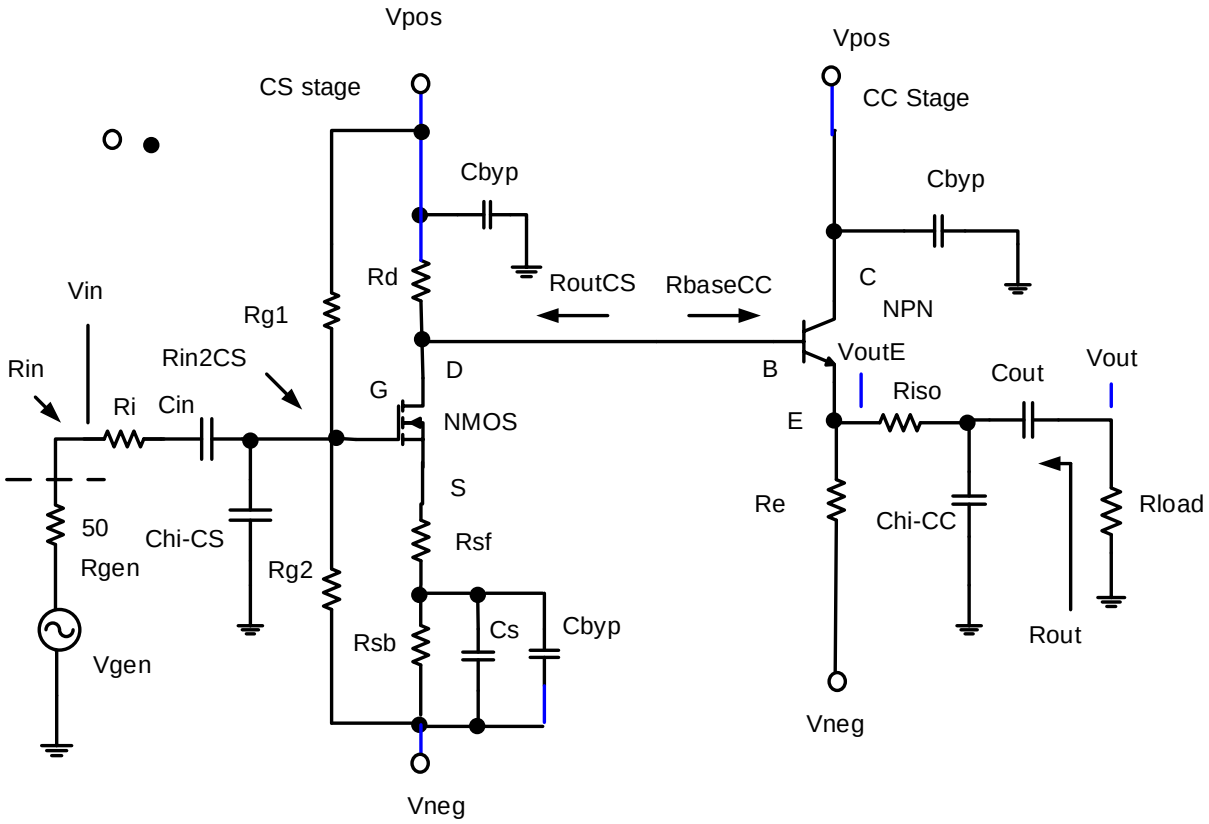
The Two-stage amplifier will combine two amplifiers that we have already designed with some changes. We will start with the output requirement as before with the Common Collector CC as the output stage. The Common Source CS will be the input stage. the CC stage and the Input and output voltage dividers all have a voltage gain of less than one. Therefor the CS stage must provide the gain we need and overcome the other stage low gain.

The Q-point for the CC will about the same as before. The base bias resistors Rb1, and Rb2 will not be use because the Common Source MOSFET CS stage drain voltage will be the voltage biasing to the base of the BJT CC. Design the CC stage for maximum output voltage swing. Set the voltage across Rs on the CS stage MOSFET source to 2V.



CS-CC figure 1: Two stage amplifier

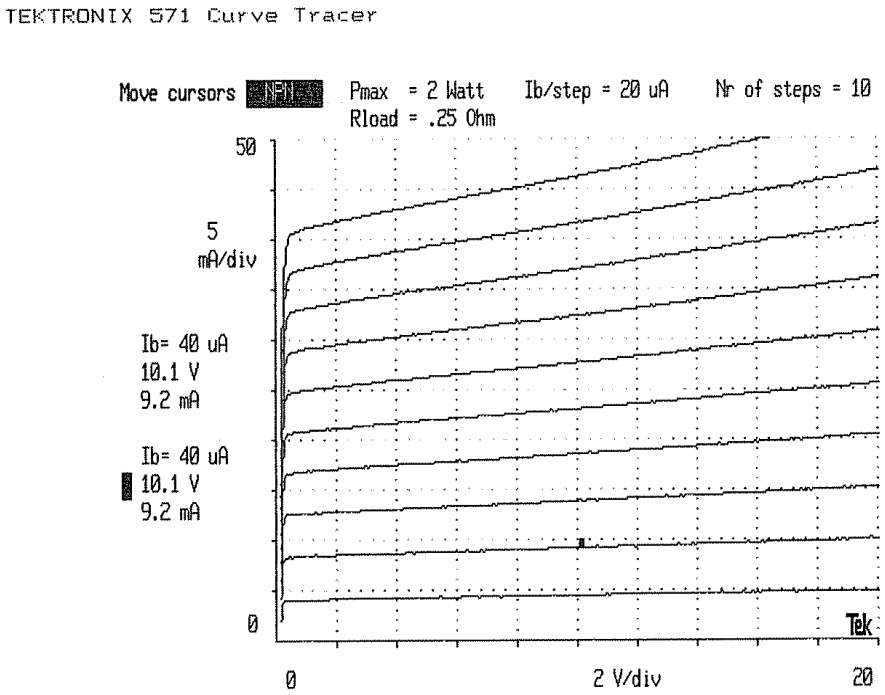
Cbyp = 0.1uF, 0.047uF, or 0.01uF

Common Collector CC Amplifier Design

Designing procedure of common collector BJT amplifier can be grouped into three systematic stages. First, we have to set the Q-point, which is the DC operating point. If the specification regarding the Q-point is not given in the design requirements; it leaves the designer enough freedom to choose the operating point as necessary for the application. However, remember that the specifications given in terms of input and output impedance, gain, frequency response characteristics and peak output voltages are tight and ultimately restricts the Q-point in a narrow window. It is difficult to analytically derive this point without some intelligent guess and the following steps would work out for the given conditions.

For common collector configuration, the circuit diagram is shown in CS_CCFig.1. The small signal equivalent model is provided in CC Fig.3.

For this configuration, same steps are involved for the calculation of R_E with few minor changes.



CC Figure 2: CC BJT curve.

CC Part 1: Measure the device parameters from the V-I curve

Step CC1.1: We need to estimate a Q-point to find an estimate for V_{CE}sat, ro and β.

For the design of the amplifier, the 3 parameter values required are V_{CE}sat, r_o and β. Derived from the transistor characteristics curve shown in CC Fig.2, one can set an approximate Q-point (V_{CE} and I_C) in the active region and measure ro and β. We will solve for V_{CE} and estimate I_C.

Solve for V_{CE} see below.

For an estimated I_C Q-point use $I_C \approx 2.6 * I_{load}$ this is not the solution to your design Q-point. We can use an estimated I_C because ro and β will not very much with small changes in Q-point.

ro = $\Delta V_{CE} / \Delta I_C$ the slope of a line thru the estimated Q-point.

β = $\Delta I_C / \Delta V_{CE}$ measured around the estimated Q-point.

Plot the estimated Q-point (V_{CE}, I_C) on the BJT characteristics curve.
From the curves CC Fig. 2 estimate V_{CE}sat the point where the curve begins to flattens out
V_{CE}sat ≈ 0.2 Vdc

CC Part 2: Find the Q-point

Use these values for the transistors: BJT, and MOSFET

For the BJT 2N3904 Use **roCC = 18 KΩ**, **β = 165, VceSat = 0.2Vdc**

For the MOSFET 2N7000 use V_{GS} = 2.1Vdc, Use **roCS = 8kΩ from your CS amp lab, VdsSat = 1.0Vdc** and **gm = 0.007**

Step CC2.1: Derive VRe Q- point

We have 2 choices how to set the VRe q-point voltage.

Use a give Vre = 5Vdc

1, Set the **VRe** to the midpoint between the V_EMax and the V_EMin. **Step CC2.1.1:**

2. Set the **VRe** to a preferred voltage tween the maximum and minimum. **Step CC2.1.2:**

Step CC2.1.1: Set VRe to the midpoint

Iload = Vout / Rload

Output signal at the emitter VoutE.

VoutE = Vout + Iload *Riso the AC signal voltage at the emitter of the BJT.

Note: The AC signal at the emitter must be higher than the output voltage Vout because of the voltage drop across Riso

V_{CE}sat = 0.2V

VReMax = Vcc – V_{CE}sat – (VoutE + 20%VoutE)

VReMin = Vee + VoutE + 20%VoutE

VRe = (VReMax + VR_EMin) / 2 Mid-point VRe Q-point

Step CC2.1.2: Choose or given the VRe voltage the voltage across Re

Iload = Vout / Rload

Output signal at the emitter VoutE.

VoutE = Vout + Iload *Riso the AC signal voltage at the emitter of the BJT.

Note: The AC signal at the emitter must be higher than the output voltage Vout because of the voltage drop across Riso

V_{CE}sat = 0.2V

VReMax = Vcc – V_{CE}sat – (VoutE + 20%VoutE)

VReMin = Vee + VoutE + 20%VoutE

Check to make sure the chosen or given VRe is between VReMax and VReMin.

Step CC2.2: Find the values of Re, I_E, and I_C
VoutE = Vout + Iload *Riso
The DC equation: VRe = Re I_E
The AC equation: Voute = i_e (Re || roCC ||(Riso + R_{Load})
Substituting VRe for i_e * Re, and the parallel calculation of the product over the sum

Combined equation: Voute = VRe (roCC ||(Riso + Rload)) / (R_E + (roCC ||(Riso + Rload)))
Rearrange combined equation

$$R_E = \frac{VR_E}{V_{outE} + 20\%V_{outE}} (r_{OCC} \parallel (Riso + R_L)) - r_{CC} \parallel (Riso + R_L)$$

Calculate I_E
I_E = VRe / Re
Calculate I_C
Ic = I_E (β / (β + 1)) use β from data sheet β = from curves or given

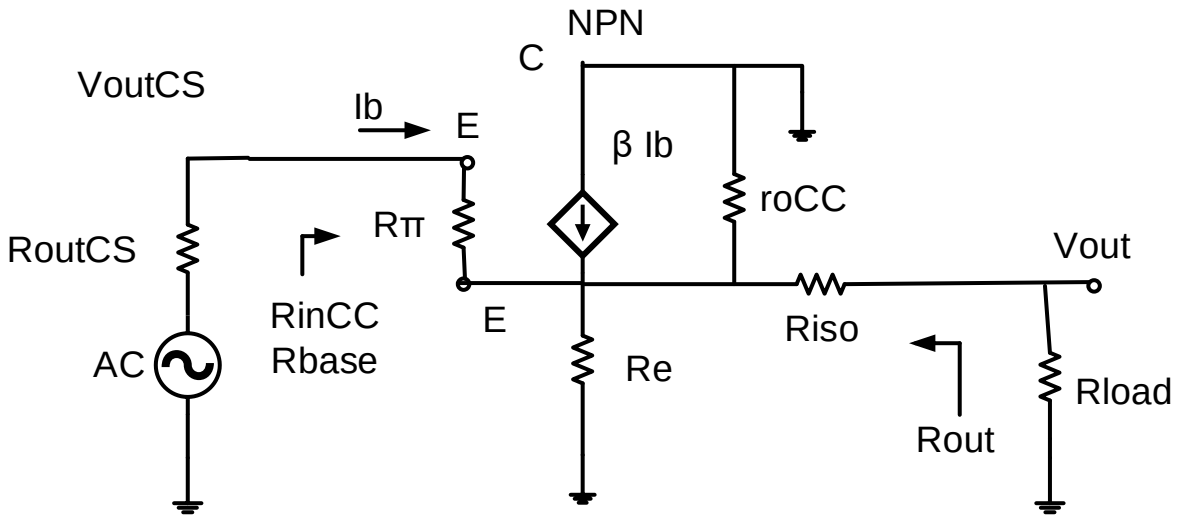
CC Part 3: Find Vb, and Vd

Step CC3.1: Calculate V_B and V_D

Vb = VRe + Vbe Q - point values

Vb will be used as the V_D Q-point voltage for the CS stage

Vd = Vb from the CC stage



CC Figure 3: Small signal equivalent model for common collector model

CC Part 4: Calculate RinCC, and Rout

Step CC4.1: Input Impedance of CC

Use β from data sheet β = from curves or given.

Rπ = β vt / Ic

Rbase = Rπ + (β + 1) ((roCC || R_E || (Riso + Rload))) Impedance looking into CC BJT base.

RinCC = Rbase

RloadCS = RinCC The load on the CS stage will be the input impedance of CC stage

Step CC4.2: CC output Impedance RoutCC: Calculate in CS-CC section **Step CS-CC1.2:**

Step CC4.3: Calculation of AvCC Voltage Gain

Derive AvCC

VoutE = i_b (β + 1) (Re || roCC || (Riso + Rload)) AC signal voltage at the emitter.

Vout = VoutE * (Rload / (Rload + Riso)) this is voltage divider of Riso and Rload

AC signal voltage at input to CC stage VinCC = VoutCS

VinCC = Rπ i_b + i_b (β +1) (R_E || roCC ||(Riso + Rload)) Voltage drop form i_b into the base.

VinCC = i_b (Rπ + (β+1) (R_E || roCC ||(Riso + Rload)) AC signal voltage at input to the CC stage.

AvCCe = VoutE / VinCC = (β+ 1) i_b (R_E || roCC || (Riso+Rload) / i_b (Rπ + (β+1) (R_E || roCC ||(Riso + Rload)))

Canceling out i_b

Voltage gain of CC base to emitter

AvCCe = (β + 1)(R_E || roCC ||(Riso + Rload) / (Rπ + (β+1)(R_E || roCC ||(Riso + Rload)))

Gain with added **output voltage divider**.

Over all Av of CC stage

AvCC = (AvCCe) (Rload / (Rload + Riso)) Gain form base to load resistor

Thus, the voltage gain should be close to 1. Hence, the output follows the input. So, the Common collector configuration is also known as Emitter follower.

Step CC4.4: Calculation Ai Current Gain

AiCC = AvCC (RinCC / Rload)

Step CC4.5: Find AC VinCC

AC signal VinCC needed produce the Vout
VinCC = Vout / AvCC AC signal voltage Vout is the peak output voltage required.

Step CC4.6: Calculate the Minimum and Maximum Vd

Need Check that Vb is between VdMax and VdMin

Chose voltage across Rs (V_{RS}) between 2.0Vdc and 3.0Vdc. The Q-point Vs = Vneg + V_{RS}

We will add 20% to VinCC so the design is not on the edge of the solution.

VinCC is the output voltage from CS stage required to drive the CC

$V_{D(max)}$ = Vpos - (VinCC + 20%VinCC)

$V_{D(min)}$ = V_S+V_{DS} sat + (VinCC + 20%VinCC)

Check $V_{D(min)} < V_B < V_{D(max)}$ DC voltage Bias point.

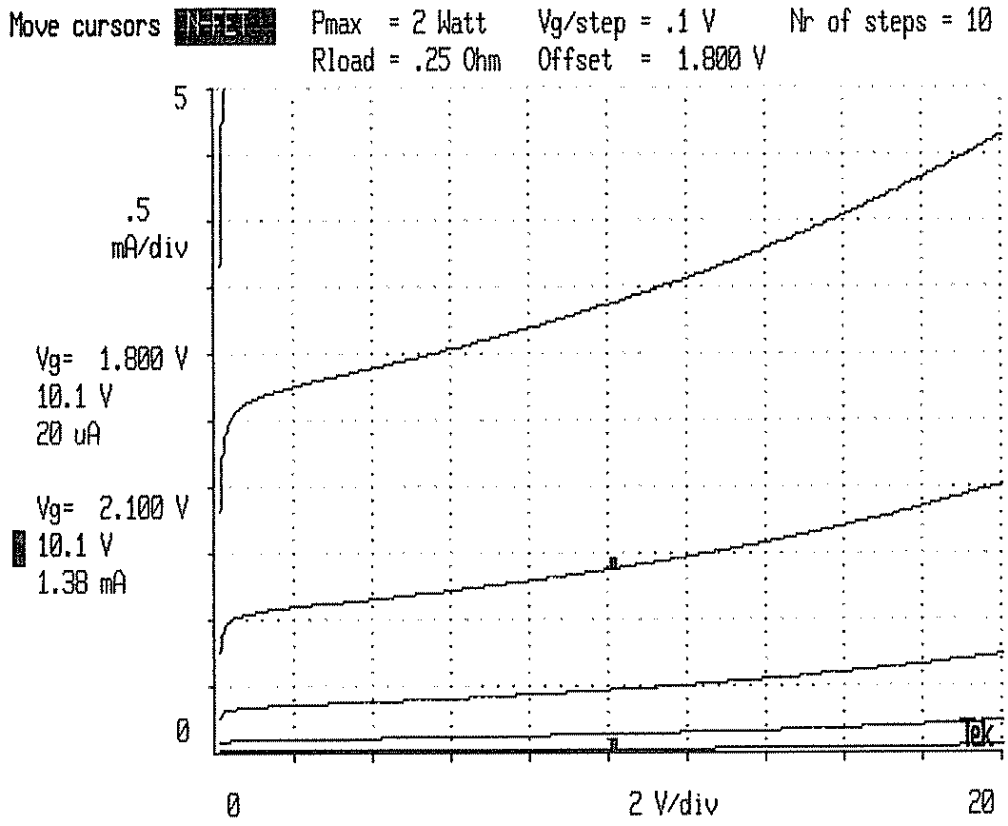
If V_B is not within CS V_D range, we will need to adjust the CC Q-point.

Common source (CS)

Designing procedure of common source MOSFET amplifier can be grouped into three systematic stages. First, we have to set the Q-point, which is the DC operating point. Since, no specification regarding the Q-point is mentioned in the design requirements, it leaves the designer enough freedom to choose the operating point as necessary for the application. However, remember that the specifications given in terms of input and output impedance, gain, frequency response characteristics and peak output voltages are fairly tight and ultimately restricts the Q-point in a narrow window. It is difficult to analytically derive this point without some intelligent guess and the following steps would work out for the given conditions.

Common Source with Source Resistance Rsf, Rsb Configuration

In this configuration, R_S is partially bypassed. The circuit diagram with necessary variables is provided in CS-CC figure 1. Rs = Rsf +Rsb



CS Figure 2: MOSFET characteristics, Example not your Q-point

CS Part 1: Measure the device parameters

For the design of the amplifier, the 4 parameter values required are Vds_{sat}, V_{GS}, r_o and gm. Derived from the transistor characteristics curve shown in CS Fig.2, one can set an approximate Q-point (V_{DS} and I_D) in the active region and measure ro and gm. We will solve for V_{DS} and estimate ID.

Solve for V_{DS} see below.

RinCC is the load seen by the CS amplifier. Where **VinCC** is the AC signal required by the CC stage to produce the required Vout.

VinCC = Vout / Av_{CC}

IloadCS = VinCC/ RinCC = (Vout/AvCC) / Rin_{CC}

Step CS1.2: Choose I_D estimate.

For an approximate I_D Q-point use $I_D \approx 3.0 * I_{load}$ peak this is not the solution to your design I_S Q-point. We can use an approximate I_D because ro and gm will not change very much with small changes in Q-point.

ro = $\Delta V_{DS} / \Delta I_D$ the slope of a line thru Q-point use **roCS = 8k** to match LTspice

gm = $\Delta I_D / \Delta V_{GS}$ measured around Q-point use **gm = 0.007** to match LTspice

Plot the estimated Q-point (V_{DS},I_D) on the MOSFET characteristics curve.
From the curves estimate V_{DS}sat the point where the curve begins to flattens out (beyond the triode region**) $Vds_{sat} \approx 1$ Vdc and $V_{GS} \approx 2.0$Vdc**

CS Part 2: Determine the Q-point.

Use these values for the transistors: BJT, and MOSFET

For the BJT 2N3904 Use **roCC = 18 KΩ**, **β = 165, VceSat = 0.2Vdc**

For the MOSFET 2N7000 use V_{GS} = 2.1Vdc, Use **roCS = 8kΩ from your CS amp lab, VdsSat = 1.0Vdc** and **gm = 0.007**

Start with your MOSFET and selecting 4 resistors.

Step CS2.1: Choose VRs Voltage across Rs

Set V_{RS} = between 2V to 3V the voltage across Rs.

If **given a value** use it for VRs

Vs = Vss + VRs

Step CS2.2: Check the range of Vd.

Check range of V_D selection will be able supply the required base voltage for the CC amp.
We will add 20% to VinCC so the design is not on the edge of the solution.
Where VinCC is the AC signal required by the CC stage to produce the required Vout.
VdMax = Vdd - (VinCC + 20%VinCC)
VdMin = VRs + Vss + VdsSat + (VinCC + 20%VinCC)
Check that the Vd = Vb is between VdMax and VdMin.

Vds = Vd – Vs Q-point Vds

Step CS2.3: Calculate Rd.

Vd and VoutCS from VinCC (required input to CC) see above Step CC4.5:

Vd = Vb Q-point Vd DC voltage
VoutCS = VinCC AC signal voltage
RloadCS = RinCC
IinCC = the larger of **Ib or VinCC / RinCC**
IloadCS = IinCC VinCC is AC input signal voltage to CC, IinCC is the Iload for CS

The DC equation: VRd = Vdd – Vd = Rd * (Id + IloadCS) Voltage across Rd
The AC equation: VoutCS = (Id + IloadCS) *(Rd || roCS || RinCC)
Substitute VRd for Rd * (Id + IloadCS)
Combined equation: VoutCS = VRd (roCS || RloadCS) / (Rd + (roCS || RloadCs))

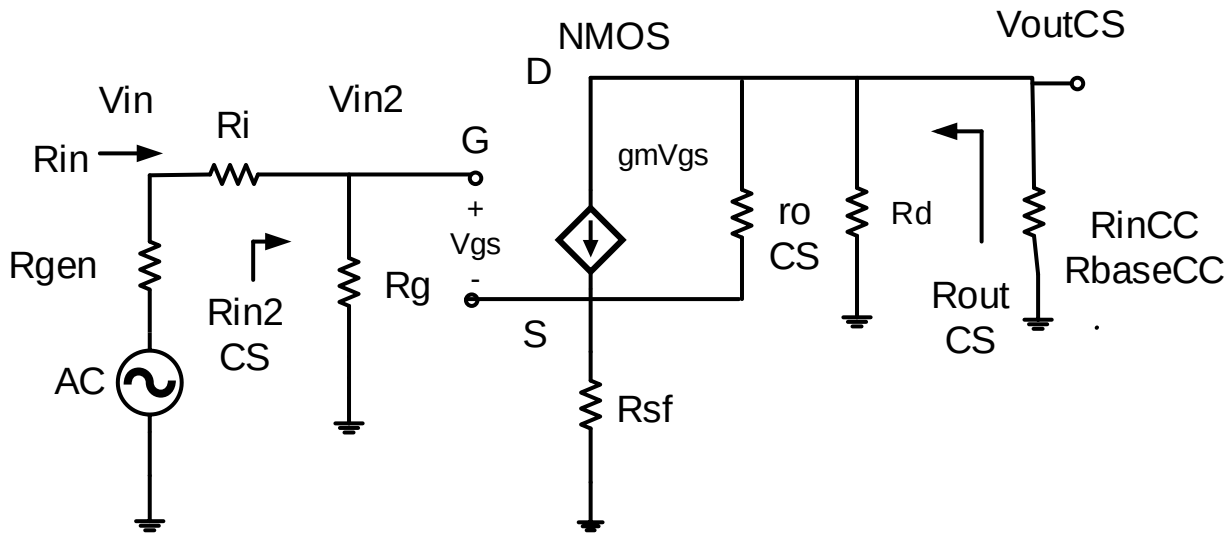
Rewriting to solve for Rd.

$$\mathrm{Rd} = \frac{\mathrm{V_{Rd}}}{\mathrm{V_{outCS}} + 20\%\mathrm{V_{outCS}}} \left(\mathrm{roCS} \parallel \mathrm{R_{LoadCS}}\right) - \left(\mathrm{roCS} \parallel \mathrm{R_{LoadCS}}\right)$$

Step CS2.4: Calculate Id.
IRd = Id + IloadCS = (Vdd – Vd) / Rd = Vrd/Rd
Id = IRd – IloadCS

Thus, Q-point is (Vds,Id).

Step CS2.5: Find V_{GS}, and V_G
Plot the Q-point (V_{DS},I_D) on the MOSFET characteristics curve.
From the curves, find V_{GS}. Use **V_{GS} = 2.1Vdc**
$V_G = V_S + V_{GS}$



CS Figure 3: Common Source Small Signal Equivalent Circuit

CS Part 3: Determine CS bias resistors.

Step CS3.1: Calculate total Rs = Rsf + Rsb.

$I_S = I_D$

$\therefore R_S = \frac{V_S}{I_S}$

Step CS3.2: Calculate R_{g1}, R_{g2}.

Set Rin to desired value

Vg = Vss + (Vgs +VRs) DC bias point

Rin desired = RinW

Rin2W = RinW – Ri

Rg1 = (Vdd – Vss) / (Vg - Vss) Rin2W

Rg2 = (Rg1 * Vg) / (Vdd – V_G)

Check Rin meets requierments

Rin2 = Rg = Rg1 || Rg2

Rin = Ri + Rin2

CS Part 4: Voltage Gain of CS stage

If open Loop **Rbs = Rs , Rsf = 0.** Skip to **CS-CC Part 1:**

Step CS4.1: Solve for Voltage Gain of CS stage need to meet overall Av.

Voltage of **output voltage divider** from VoutE to Vout.
Vout/ VoutE = **AvOutputDivider = Rload / (Riso + Rload).**

Voltage of **input voltage divider** from Vin to Vin2.
Vin2/Vin = **AvInputDivider = Rin2 / (Ri + Rin2)**.

AvCCe base to emitter = (β + 1)(R_E || roCC ||(Riso + Rload) / (Rπ + (β+1)(R_E || roCC ||(Riso + Rload))).

Av overall voltage gain required.

AvCS2 the voltage gain of CS stage required to give us the overall voltage gain.

AvCS2 = Av / (AvOutputDivider * AvCCe ***** AvInputDivider)

VoutCS = - gm v_{gs}(Rd || roCS || RinCC)

Vin2 = v_{gs} This is not the DC Q-point voltage, v_{gs} = AC input voltage signal on the gate if Rsf =0.

Vin2 = v_{gs} + (gm v_{gs}) * Rsf = v_{gs} (1 +gm Rsf) if Rsf > 0.

Voltage gain at Vin2 to VoutCS of CS stage, this is without the input voltage divider.

AvCS2 = VoutCS / Vin2 = (- gm (R_D || (r_oCS + (Rsf || 1/gm)) || RinCC)) / (1 +gm Rsf)

Step CS4.2: Solve for Rsf that set the required gain of the CS stage.

Set the Rsf so the gain of the CS stage meets the require gain.

The full equation can be simplifier Note: AvCS2 is negative.

Rsf = - (Rd || RinCC || (**r_oCS + (Rsf || 1/gm**))) / AvCS2)) - 1 / gm

We do not have Rsf yet so we will approximate the term

roCS + (Rsf || 1/gm) ≈ roCS

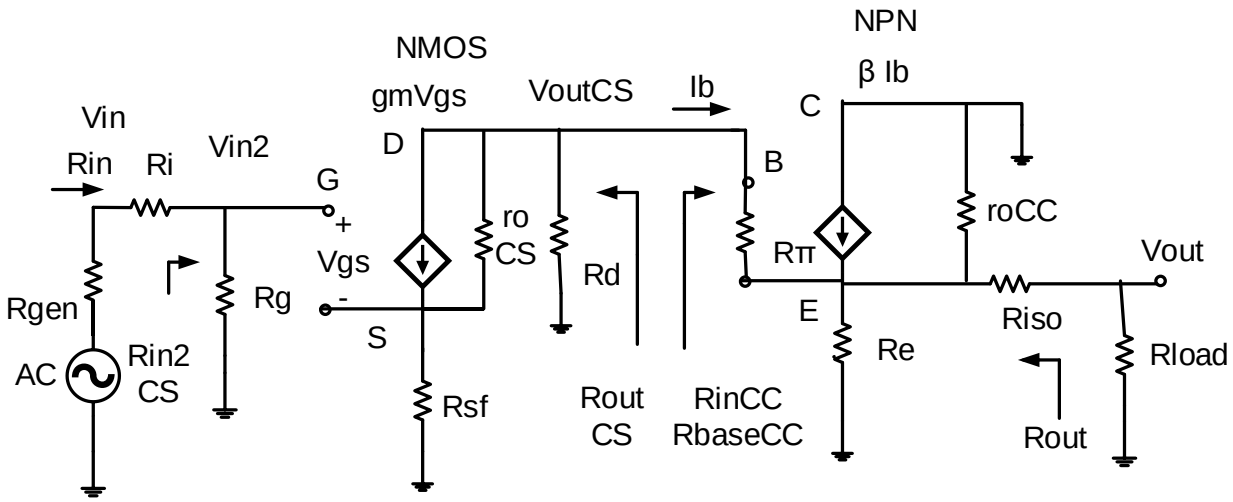
Yielding : Note: AvCS2 is the desired Voltage gain of CS amp from Vin2 to VoutCS

Rsf = -((Rd || RinCC || r_oCS) / AvCS2) - 1/gm

Rsb = Rs – Rsf

CS-CC Part 1: Calculating impedance and Gain

Refer to the small signal equivalent of the circuit you have just built in CS-CC Fig. 4. The capacitor values calculated in the next step. We can calculate the following:



CS-CC Figure 4: Two stage Small Signal Equivalent Circuit

Step CS-CC1.1: Input Impedance: CS-CC

CS stage

Rin2CS = Rg = R_{g1} || R_{g2}

CC stage

RbaseCC = RπCC + (β + 1) ((roCC || R_E || (Rload + Riso))) Impedance looking into BJT base.

RinCC = RbaseCC

CS-CC input impedance

Rin = Rin2CS + Ri Input impedance of two stage amplifier.

Step CS-CC1.2: Output Impedance: CS-CC

Output Impedance of CC taking in the effect of the CS stage RoutCC

RemitterBase is the impedance looking in the BJT emitter to base.

RoutCS = Rd || roCS CS stage, Rs completely bypassed by Cs

RemitterBase = (RπCC + RoutCS) / (β + 1) Look into the CC emitter, note we will see the RoutCS of the CS.

RoutCC = Riso + (R_E || roCC || RemitterBase) output impedance of the CC stage.

CS Stage

If **Rsf = 0** open loop AvCS then

RoutCS = Rd || roCS impedance looking CS stage

If **Rsf is greater than zero** then controlled AvCC voltage gain.

RoutCS = Rd || (roCS + (Rsf || (1/gm)) impedance looking CS stage

CC stage

Referring to small signal model CC Fig.3, let us find Vout / VinCC, which would be a key step in calculating Av.

RemitterBase = (RπCC + RoutCS) / (β + 1) Impedance looking into the emitter thru RπCC.

RoutCCe = Re || roCC || RemitterBase Output impedance at the emitted without Riso

CS-CC Output impedance overall amplifier

RoutCC = Riso + (Re || roCC || RemitterBase) Overall output impedance.

Rout = RoutCC The output impedance of the two stage amplifier. Includes the calculations from both stages.

Step CS-CC1.3: Voltage Gain

AvCS-CC = Vout / Vin overall voltage gain

AvOutputDivider = Rload / (Riso + Rload)

AvInputDivider = Rin2 / (Ri + Rin2)

Voltage gain from VinCC to VoutE **AvCCe = VoutE / VinCC.**

AvCCe = (β + 1)(Re || roCC ||(Riso + Rload) / (Rπ + (β+1)(R_E || roCC ||(Riso + Rload))).

Voltage gain CS from gate **Vin2** to output of CS **VoutCS**

AvCS2 = VoutCS / Vin2 = (- gm(Rd || RinCC || (roCS + (Rsf || 1/gm)))) / (1 + gm Rsf)

Total amplifier voltage gain AvCS-CC

AvCS-CC = Vout/Vin = AvInputDivider * AvCS2 * AvCCe * AvOutputDivider

Step CS-CC1.4: Current Gain
Total amplifier current gain AiCS-CC

AiCS-CC = Iload / Iin = AiCS * AiCC = AvCS-CC (Rin /Rload)

AiCS-CC = AvCS-CC (Rin /Rload)

Step CS-CC 1.5: Power gain GdB

G = Pout / Pin = Vout * Iload / Vin * Iin = AvCS-CC * AiCS-CC

In decibels GdB = 10Log(G) = 10log (AvCS-CC * AiCS-CC)

Step CS-CC 1.6: Calculate Vin and Voc of VgenOC
Input signal level need to produce the required output voltage.
Vin = Vout / AvCS-CC

The open circuit voltage of the generator to produce the required output voltage.
Because of Voltage divider because the output impedance of the Rgen = 50Ω

VgenOC = Vin (Rgen + Rin) / Rin Set this value in function generator.

Use this value in LTspice and the laboratory Function generator

CSwRsf Step 4.6: Vin and Voc of Vgen
Input signal level need to produce the required output voltage.
Vin = Vout / AvCS-CC

The open circuit voltage of the generator to produce the required output voltage.
Voltage divider at the input because the output impedance of the is Rgen = 50Ω

VgenOC = Vin (Rgen + Rin) / Rin Set this value in function generator.

Use this value in LTspice and the laboratory Function generator

Frequency response of Two Stage CS – CC amplifier

CS-CC Part 2: Frequency response

With the Q-point being set after the sequence of steps, we can go for the selection of capacitors and finally connect the signal generator at input and measure the output amplified waveform.

Step CS-CC2.1: Set low frequency cutoff break points

Select C_{in}CS, C_{out}CC and C_S which jointly would set the roll-off beyond the lower cut-off frequency. Set any low frequency cutoff (F_L) within the range as your lower cut-off frequency

range requirement. Three capacitors will introduce 3 poles in the transfer function of the system. Because we will set 3 pole at the same frequency we must use the Band Width Shrinkage factor.

$$\text{BWshrinkage} = \sqrt{2^{\frac{1}{n}} - 1}$$

Where n is the number of poles for low frequency breakpoints at same frequency.

$$f_L = \frac{f_{C_{in}} + f_{C_{out}} + f_{C_E}}{3\sqrt{2^{\frac{1}{3}} - 1}}$$

Setting 3 frequencies equal, we get, n= 3

$F_{Cin}CS = F_{Cout}CC = F_{CS} = F_L \sqrt{2^{1/3} - 1}$

Find the C for each breakpoint f_{Cin} , f_{Cout} , and f_{CS} where n = 3.

$$C = \frac{1}{2\pi f_C \,(\text{R seen by C})}$$

Where C is the capacitor that sets the breakpoint f_C

R is the Thevenin equivalent resistance seen by the capacitor.

R_{Cin} = Ri + Rgen + Rin2CS

R_{Cs} = Rs || (Rsf + (roCS + R_D || RbaseCC) || (1 / gm))

Rc_{out} = Rout + Rload

Step CS-CC2.2: Set high frequency cutoff break points

In this case because ChiCS, and ChiCC are set to the same break point. We must use the band shrinkage factor with n = 2. We need only to find a two zeros at F_h / bandshrinage = $f_{chi} = f_{ch2}$ to set the high frequency cutoff.

Set FchiCS = FchiCC = Fh / $\sqrt{2^{1/2} - 1}$

ChiCS

RChiCS = (Rgen + Ri) || (Rg1 || Rg2) impedance ChiCS sees.

$$C_{hiCS} = \frac{1}{2\pi f_{ChiCS}\,(\text{R seen by } C_{hiCS})}$$

ChiCC

R seen by C_{hiCC}

Looking into the CC emitter, note we will see the Rout of the CS.

RemitterBase = (Rπ + RoutCS) / (β + 1) RemitterBase is the resistance seen looking into the emitter towards the base.

RoutCC = (R_E || roCC || RemitterBase) + Riso looking in to the CC stage.

R_{Chi}CC = RoutCC || Rload

$$C_{hiCC} = \frac{1}{2\pi f_{Chi2}\,(\text{R seen by } C_{hiCC})}$$

The following table enlists the particular expressions.

C_{in}	Rgen + Ri + Rin2CS
Cout	RLoad + RoutCC
C_S	Rsb || (Rsf +(roCS + (R_D || RinCC)) || (1 / gm))
C_{hi}CS	(Rgen + Ri) || (Rg1 || Rg2)
C_{hi}CC	RoutCC || Rload

CS - CC Table 1: Resistance Seen By Capacitors