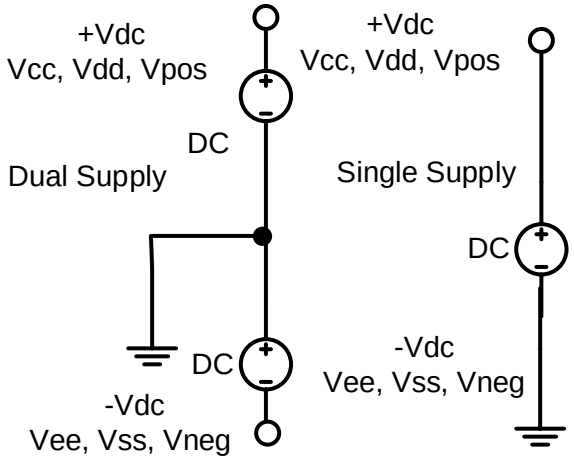
ECE 3274
Common-Emitter Amplifier Project

1. Objective

The objective of this lab is to design and build the common-emitter amplifier with partial bypass of the emitter resistor to control the AC voltage gain Av. We will use a single supply in the lab classroom if in person.



2. Components

Qty	Device
1	2N3904 BJT Transistor

3. Introduction

One of the most popular single-transistor BJT amplifier designs is the common emitter (CE) amplifier design. The CE amplifier is relatively simple to bias, delivers a high voltage gain, and is easy to understand. In this lab, you will design and build such an amplifier. The procedure for this lab is straightforward. First, you will design a controlled gain amplifier for your prelab assignment. This process will involve designing the 4-resistor bias circuit and tailoring the frequency response of the amplifier circuit to meet the requirements. **Hint**: design for the Vout peak voltage and input resistance Rin. Then you will build the amplifier in the lab and test it to see whether it meets the requirements.

You should refer to your lab lecture notes, your Electronics II Lecture notes, your textbook, the course website, and other reference material to determine how best to design your amplifier. This lab is intended as a design project and not as a step-by-step guide.
Use BJTAmpDesignCE link.

4. Requirements

Your amplifier design must meet the following requirements.

Requirement	Specification
Voltage Gain (Reb Bypassed)	$\|A_v\|$ = Between 3V/V and 5V/V
Low Frequency Cutoff (FL)	Between 100 Hz and 300 Hz
High Frequency Cutoff (FH)	Between 75 kHz and 150 kHz
Input Impedance	Between 2KΩ and 5KΩ
Output Voltage	$2.0V_P$
Load Resistance	2.2 kΩ
Total Emitter Resistance	Two Resistors, $R_e = R_{ef} + R_{eb}$
Power Supply Voltage	Single Vcc = $12V_{dc}$ Vee = $0V_{dc}$

Table 1. Common-emitter amplifier requirements.

5. Prelab Design Project

You will design an amplifier in this prelab design project. The design will make use of a partially bypassed emitter resister Reb, and an emitter bypass capacitor Ce, thus controlling the gain and input impedance of the amplifier. The values of the capacitors will also change from design to design. **Units must be included** as well it is permissible to include a table of final values for clarity if you would prefer, but again, all work must be **handwritten**.

Use the following fixed component values in your circuit:

Component	Value
R_i	150Ω
C_{byp} **Choose a value** **They will all work**	0.1µF 0.047uF 0.01uF

Table 2. Fixed component values.

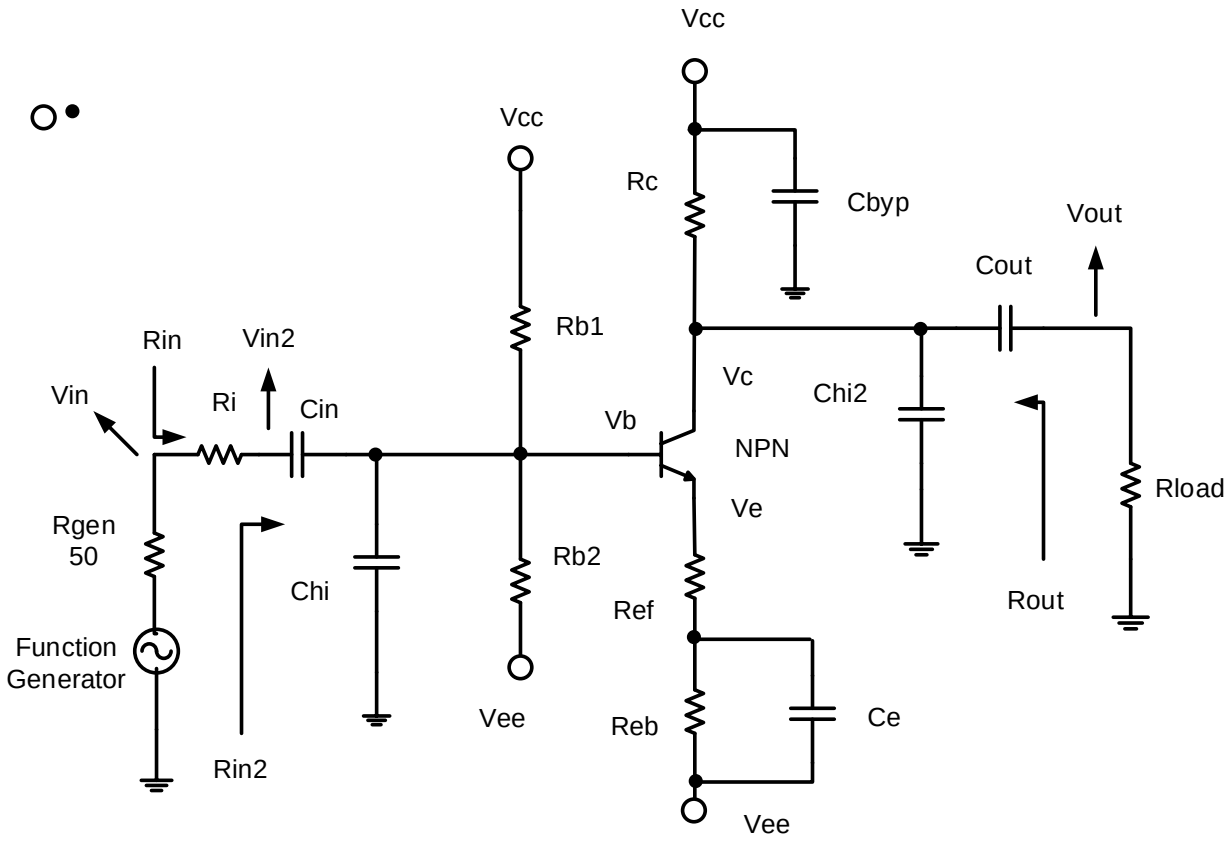


Figure 1. Common-emitter amplifier circuit. Re = Ref + Reb

5.1 DC Bias

Begin by designing the Q-point based on the output and input requirements. Use this to design the DC bias for the amplifier. The emitter resister Re is the sum of the two emitter resisters the unbypassed Ref and the bypassed Reb emitter resister. The values of these resisters will control the Voltage Gain (Av) of the amplifier. Note that the location and value of the capacitors do not affect the biasing, so the values you calculate here will be valid for the amplifier Q-point design. Once you have designed the DC bias, use the transistor characteristics for the 2N3904 transistor to determine the transistor parameters (β, ro, Vce_sat) for where you are operating. Note that there is no single correct answer and that your design may differ significantly from your colleagues. You must show all your work and walk through all calculations.

Choose the sum of the voltage drop across $V_{REF} + V_{REB}$ to be between **2v and 3V**.

$V_E = Vneg + V_{REF} + V_{REB}$

$V_B = V_E + V_{BE}$

Rin=Ri + Rin2.

If you need to set the input impedance to a required value.

Set Rin2 = Rin – Ri

Rin2 = Rb1||Rb2|| [r_π +(β+1){Ref|| (ro + Rc||Rload)}] CE with Ref
V_B = Vcc*(Rb2/(Rb1+Rb2)).
Solve for Rb1, and Rb2

Component Values	Amplifier Parameters	Voltages and Currents
R_{b1}	Beta DC From curve	V_{ce}
R_{b2}	Beta AC From curve	V_{be}
R_c	r_π	V_e
R_e	r_o From curve	I_b
		I_c

Table 3. DC Bias and Amplifier Parameters

5.2 AC: Design
We will now design and calculate the AC characteristics for the partially bypassed CE amplifier, with the emitter capacitor, bypassing Reb. Resistor Ref is not bypassed and provides negative feedback for the AC signal. **Table 4** shows all of the values you need to calculate. Be sure to show all work. You may use the equations given in the lab lecture and design reference, a word of caution some of the outside references will use approximations. Be sure you understand how to use the equations, though if assumptions are included, you must state these and show that you meet them.

For the FL low frequency cut off.
We will set all 3 break points (n=3) to the same frequency this causes band spreading so FL = Fcin + Fcout + Fce will be incorrect. We will use a break point frequency for each capacitor of FL'.

$FL' = FL * \sqrt{2^{(\frac{1}{n})} - 1}$ For each capacitor (Cin, Cout, Ce) use C=1 / (2 π FL' Req)
Where Req the equivalent resistance across the capacitor.

$BWshrinkage = \sqrt{2^{1/n} - 1}$ Where (n = 3) is the number of low frequency zeros at the same frequency.
FL = (Fcin + Fcout + Fce) / (BWshrinkage*n) if all 3 break points (n=3) at the same frequency Fcin = Fcout = Fce = FL * BWshrinkage

For the FH High frequency cut off.
$BWshrinkage = \sqrt{2^{1/n} - 1}$ Where (n = 2) is the number of high frequency poles at the same frequency. FH' = FH / (BWshrinkage)
Chi, and Chi2 control the high frequency cutoff and will help prevent high frequency oscillations.
$FH' = \frac{FH}{\sqrt{2^{(\frac{1}{n})} - 1}}$ Where (n = 2) is the number of high frequency poles at the same frequency.
Chi, Chi2 = 1/(2 π FH' Req). Where Req the equivalent resistance across each capacitor.

5.3 AC: Gain of a Partial Emitter Bypass CE amp

Capacitor C_e only bypassing Reb and Re = Ref + Reb. The gain will be lower than if we bypassed both Ref and Reb.

$$Av2 = -\frac{\beta R_L'}{r_\pi + (\beta+1)R_{ef}}$$ Where and R_L' = Rc||R_L

Component Values	Amplifier Parameters	Voltages, Currents, and Power
C_{in}	Voltage Gain	v_{in}
C_{out}	Current Gain	v_{out}
C_e	Power Gain (in dB)	i_{in}
C_{hi}	Low Frequency Cutoff	i_{out}
	High Frequency Cutoff	p_{in}
	Input Resistance	p_{out}
	Output Resistance	

Table 4. Small Signal (ac) Amplifier Parameters

5.4 Computer-aided Analysis (25 Points)

Once you have completed your amplifier design, use a circuit simulator LTspice to analyze their performance. Note: **Must include LTspice schematics and plots must be labeled**. Generate the following plots for the amplifier design:

- **(a)** A time-domain plot of the input and output, with the output voltage at the (Vout) of the design requirement or greater at 5 kHz. The output should not have any distortion or clipping. Calculate the midband gain and indicate it on the plot. Compare this to your calculated values.
- **(b)** An FFT of your time-domain waveform. Circle and indicate the height of any strong harmonics, in dB relative to your fundamental frequency at 5 kHz.
- **(c)** A frequency sweep of the amplifier from 10 Hz to 1 MHz Indicate the high and low frequencies cutoffs on the plot (these should correspond to the half-power, or 3dB below midband). Compare these to your calculated values.

5.5 Prelab Question

How could you vary the gain of the amplifier by using a potentiometer of a value equal to sum of R_{ef}, and R_{eb} without affecting the Q point? Draw a circuit.

6. Lab Procedure

6.1 Construct the CE amplifier shown in Figure 1. Must bypass the power supply on your proto board with a 0.1uF, 0.047uF or 0.001uF capacitor to prevent oscillations.
Remember that R_{gen} is internal to the function generator and is not in your circuit. Remember to use the two emitter resistors values from your design.
Record the values of the bias network resistors and the capacitors you used in the circuit.

6.2 Measure the following values: Measure at undistorted output.

(a) Q-point: Vc, Vb, Ve, Vce, Vbe, Ie, Ic, and Ib Note: Ib = Irb1 – Irb2.
Use DC multimeter measure from the reference point the ground between the two power supplies. Note: Calculate the current from a voltage across a resister.

Hint: If your Q-point Vb, Vc, and Ve are not as expected. Remove the BJT and measure Base, Collector and Emitter nodes. Vb = expected bias voltage, Vc = Vcc, and Ve = Vee.

(b) Voltage, current, and power gains. AC multimeter at 5kHz.

(c) Maximum undistorted peak-to-peak output voltage measured at 5kHz. Use scope.

(d) Input and output resistance measured at 5kHz. Note use Ri to calculate Iin.Use AC multimeter.

(e) Low and high cutoff frequencies (half power point).From frequency response plot use scope.

Recall that input impedance is given by $R_{in} = v_{in}/i_{in}$, output impedance is given by $R_{out} = (v_{oc}-v_{out})/i_{Load}$, voltage gain is given by $A_v = v_{out}/v_{in}$, and current gain is given by $A_i = i_{Load}/i_{in}$.

Additionally, plot the following: 4 plots

(a) Input and output waveform at the maximum undistorted value.

(b) FFT of Vout showing the fundamental and first few harmonics of signal Vout use the **scope**.

(c) Frequency response from 10 Hz to 1 MHz (set the input voltage to a value that does not cause distortion across the entire passband of the amplifier).

6.3 Replace the load resistor, Rload, with a 100 Ohm and a 10k resistor, and at 5kHz input adjust the Vin level to obtain the maximum output peak to peak voltage without clipping and measure the voltage gain Av. Comment on the loading effect, and remember to change back to a **the original load resistor** after this step.

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Common Emitter Amplifier Lab
Report Data Sheet

Name: _____ **Lab Date:** _____ **Bench:** _____

Group: _____ **CRN:** _____

Remember to include units for all answers and to label all plots and a **photo** of your built circuit. There are a total of 4 plots in this lab. Submit the results online to canvas. **10 point reduction (in class only)** if in lab you do not replace all connectors, components, and cables.

6.1 Component Values Measure before building.

R_{b1}:		**R_{b2}:**		**R_c:**	
R_{ef}:		**R_{eb}:**		**R_L:**	

6.2 Common-emitter amplifier. There are 4 plots at maximum undistorted output (Vin, Vout, Power spectrum, and AC sweep). $I_B = I_E - I_C$. Use multimeter measure from the reference point ground between the two power supplies. Current is calculated from voltage across a resistor.

Capacitor Values:	C_{in}:		C_{out}:			
	C_e:		C_{hi}:			
Q-Point DC voltmeter:	V_C:		V_B:		V_E:	
	Calculate I_B:		I_C:		I_E:	
	V_{CE}:		V_{BE}:		$V_{CC:}$	
Gain AC voltmeter:	Voltage:		Current:		Power:	
Voltage Output scope:	Max:					
Resistance (AC):	Input		Output			
Cutoff Frequency:	Low:		High:			

6.3 Common-emitter amplifier at 5kHz input adjust the Vin level with a different load resistors measure with scope the maximum undistorted output. (no plots).

100Ω load resistor:

Gain:	Voltage:		Current:		Power:	
Voltage Output Vpp:	Max:					

10kΩ load resistor:

Gain:	Voltage:		Current:		Power:	
Voltage Output Vpp:	Max:					