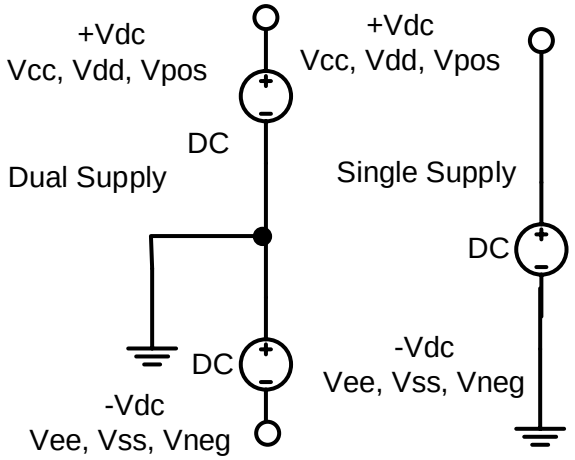
ECE 3274
MOSFET CD Amplifier Project

1. Objective

This project will show the biasing, gain, frequency response, and impedance properties of the MOSFET common drain (CD) amplifier. We will use a single supply in the lab.



2. Components

Qty	Device
1	2N7000 MOSFET Transistor enhanced N-Channel

3. Introduction

Two of the most popular configurations of small-signal MOSFET amplifiers are the common source and common drain configurations. These two circuits are shown in Figures 1 and 2 respectively. The common drain amplifier, like all MOSFET amplifiers, have the characteristic of high input impedance. The value of the input impedance for both amplifiers is limited only by the biasing resistors R_{g1} and R_{g2} for Rin <1MΩ. Values of R_{g1} and R_{g2} are usually chosen as high as possible to keep the input impedance high. High input impedance is desirable to keep the amplifier from loading the signal source. One popular biasing scheme for the CD configurations consists of the voltage divider R_{g1} and R_{g2}. This voltage divider supplies the MOSFET gate with a constant dc voltage. This is very similar to the BJT biasing arrangement described in common emitter amplifier. The main difference with the BJT biasing scheme is that ideally no current flows from the voltage divider into the MOSFET.

The CD MOSFET amplifiers can be compared to the CC BJT amplifiers. The CD amplifier is comparable to the CC amplifier with the characteristics of high input impedance, low output impedance, and less than unity voltage gain. The corner frequencies of the CD frequency response can also be approximated using the short circuit and open circuit time constant methods.

The 2N7000 MOSFET used in this project are an n-channel enhancement-type MOSFET. For the enhancement-type MOSFET, the gate to source voltage must be positive and no drain current will flow until V_{GS} exceeds the positive threshold voltage V_{TN}. V_{TN} is a parameter of each particular MOSFET and is temperature sensitive. This parameter sensitivity to temperature is one reason

for establishing a stable dc bias. The 2N7000 MOSFET data sheet lists the minimum and maximum values of V_{TN} as 0.8 V and 3.0 V respectively.

The MOSFET can be easily damaged by static electricity, so careful handling is important.

You should refer to your lab lecture notes, your Electronics II Lecture notes, your textbook, the course website, and other reference material to determine how best to design your amplifier. This lab is intended as a design project and not as a step-by-step guide.

4. Requirements

Your **common-drain** amplifier design must meet the following requirements.
Vrs is the bias voltage across the Rs resistor.

Requirement	Specification
Voltage Gain	$\|A_v\|$ > 0.4 V/V open loop
Low Frequency Cutoff	Between 100 Hz and 300 Hz
High Frequency Cutoff	Between 50 kHz and 150 kHz
Choose the Input Impedance	Between 1kΩ and 2kΩ
Set the Vrs	6Vdc
Output Voltage	$4.0V_{pp}$
Load Resistance	220 Ω
Power Supply Voltage	Single Vdd= +12Vdc Vss = 0Vdc

Table 1. Common-drain amplifier requirements.

5. Prelab Design Project

For this project, you will design the common drain amplifier with an output isolation resistor Riso. The circuit shown in Figure 1. You should refer to your class notes, textbook, instructor, and other reference material to help you design the circuits. Start with the DC design and then move onto the AC design.

Component	Value
R_i	150Ω
C_{byp}	0.1µF, 0.047uF, or 0.001uF
Riso	47Ω

Table 2. Fixed component values.

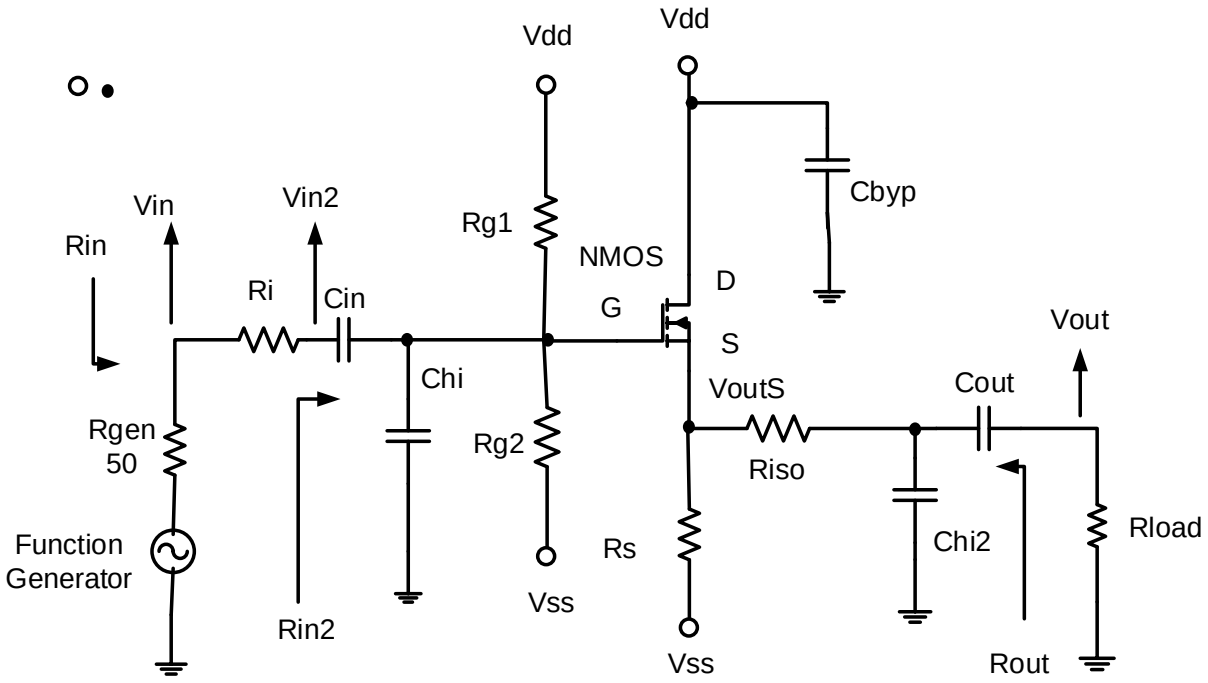


Figure 1. Common-drain amplifier circuit.

5.1 DC Bias

Begin by designing the DC bias networks for the amplifiers. You will start by examining the output requirements to select the Q-point V_{Rs}.

Vrs is the voltage across the source resister Rs.

We will start with V_{RS}(max) and V_{RS}(min).

VoutSource = Vout + I_{Load} * Riso Vout at the source (VoutS)

V_{RS}(max) = Vdd – V_{DS}sat – (VoutSource + 20%VoutSource)

V_{RS}(min) = Vss + VoutSource + 20% VoutSource

V_{RS} = (V_{RS}(max) + V_{RS}(min)) / 2 **This is the Midpoint V_{RS} Q-point use if not given**.

Vs = V_{RS} - Vss

V_{DS} = V_D – V_S

I_D estimate. = 2.6 * Iload not the actual design value.

Once you have designed Vds and the *I_D estimate*, The approximate Q-point use the transistor characteristics for the 2N7000 transistor to determine the transistor parameters from the curves for where you are operating. Note that there is no single correct answer and that your design may differ significantly from your colleagues. You should show all work and walk through all calculations. You must calculate and show all of the following values for both amplifiers (excluding R_D for the common drain amplifier).

Component Values	Device Parameters	Voltages and Currents
R_{G1}	V_{TN}	V_{DS}
R_{G2}	r_o	V_{GS}
R_S	g_m	V_S
		I_D

Table 3. DC Bias and Amplifier Parameters

5.2 AC Design

Design the ac characteristics of the amplifier. We will add an **isolation output resistor Riso** to help the drive requirements of a large capacitor load. You must calculate and show all of the following values. The high frequency cutoff is controlled by **Chi and Chi2** = 1/(2 π FH' Req). **Chi2** will help prevent high frequency oscillations. Because we will set the all poles for the high frequency break point at the same frequency.

We will use the bandwidth shrinkage formula to adjust the frequency of each pole.

$BWshrinkage = \sqrt{2^{1/n} - 1}$ Where (n) number of high frequency poles at the same frequency.

FH' = (FH) / (BWshrinkage) where n =2.

Fchi = Fchi2 = FH' Set for same break point.

Chi = 1/(2π Fchi Rchi) Chi2 = 1/(2π Fchi2 Rchi2)

The low frequency cutoff is controlled by **Cin and Cout** = 1/(2 π FL' Req). Because we will set the all zeros for the low frequency break point at the same frequency.

We will use the bandwidth shrinkage formula to adjust the frequency of each zero.

$BWshrinkage = \sqrt{2^{1/n} - 1}$ where (n) number of low frequency zeros at the same frequency.

For the CD there are 2 low frequency capacitors Cin, and Cout so use

FL' = (FL)*(BWshrinkage) where n = 2.

Fcin = Fcout = FL' Set for same break point.

Cin = 1/(2π Fcin Rci) Cout = 1/(2π Fcout Rcout)

Component Values	Amplifier Parameters	Voltages, Currents, and Power
C_{in}	Voltage Gain	v_{in}
C_{out}	Current Gain	v_{out}
	Power Gain (in dB)	i_{in}
C_{hi}	Low Frequency Cutoff	i_{out}
C_{hi2}	High Frequency Cutoff	p_{in}
	Input Resistance	p_{out}
	Output Resistance	

Table 4. Small Signal (ac) Amplifier Parameters

5.5 Computer-aided Analysis (25 Points)

Once you have completed your amplifier design, use LTspice to analyze their performance. You will need to install 2N7000 model for LTspice it is available from the class web site. Note: **Must include LTspice schematics**. Generate the following plots:

(a) A time-domain plot of the input and output, with the output voltage of at the specified output voltage of the CDamp at 5 kHz. The output should not have any distortion or clipping. Calculate the midband gain Remember the gain is **Vout/Vin**, and indicate it on the plot. Compare this to your calculated values.

(b) An FFT of your time-domain waveform. Circle and indicate the height of any strong harmonics, in dB relative to your fundamental frequency at 5 kHz.

(c) A frequency sweep of the amplifier from 10 Hz to 1 MHz. Indicate the high and low frequencies on the plot (these should correspond to the half-power, or 3dB below midband points). Compare these to your calculated values.

6. Lab Procedure

Test your 2N7000 MOSFET with the curve tracer before build your experiment.
Set curve trace to N-FET, Is Max = 10ma, Vds max =10V, Vg/step = 0.1V, Offset = 1.8V, Rload= 10, N Steps = 10
Use the 2N7000 V-I curves on the web site.

6_1. Construct the CD amplifier shown in Figure 2. Remember that R_{gen} is internal to the function generator Fgen = 5kHz. Check the power (I_S^2 Rs) in the Rs if it is greater than **250mW** to use two source resistors to equal your design value (Rs) ether in series or parallel. Record the values of the bias network resistors and the capacitors you used in the circuit. R_L = Given value. Install the Electrolytic capacitors with the correct polarity.

6_2. Measure the following values:
Turn off the function generator output when measuring the DC bias point.

(a) Q-point: V_{GS}, V_{DS}, V_S, V_G, V_D, and I_D (measure voltage across a known resister. Assume $I_D = I_S$).

Turn on the function generator output, measure at 5kHz.

(b) Voltage, current, and power gains.
(c) Maximum undistorted peak-to-peak output voltage.
(d) In the Lab only: THD% of output waveform (add distortion step)
(e) Input and output resistance at 5kHz Rin = Vin / Iin, Rout = (Voc – Vout) / I_{load}

AC sweep

(f) Low and high cutoff frequencies and BW (half power or 3dB below midband points).

Recall that input impedance is given by $R_{in} = v_{in}/i_{in}$, output impedance is given by $R_{out} = (v_{oc}-v_{load})/i_{load}$, voltage gain is given by $A_v = v_{out}/v_{in}$, and current gain is given by $A_i = i_{load}/i_{in}$.

Additionally, plot the following:

(a) Input and output waveform at the maximum undistorted value.
(b) In the Lab only: Power spectrum (add step) showing the fundamental and first few harmonics.
(b.1) At home: use FFT plot function of the scope of the Vout.
(c) Frequency response (ACsweep) from 10 Hz to 1 MHz set the input voltage (generator output) to a value that does not cause distortion across the entire passband of the amplifier.

6_3. Replace the load resistor, R_L, with a 100Ω and a 27kΩ resistor, and measure the maximum output swing and voltage gain without output clipping. Comment on the loading effect, and remember to change back to the specified load resistor after this step.

ECE 3274
MOSFET Amplifier Lab Report Data Sheet

Name:_____ **Lab Date:**_____ **Bench:**_____

Partner-Group:_____

Remember to include units for all answers and to label all printouts. There are a total of six (8) printouts in this lab. Use the 2N7000 V-I curse on the web site.

In Lab only: You must test your 2N7000 MOSFET with the curve tracer before build your experiment.
Set curve trace to N-FET, Is Max = 10ma, Vds max =10V, Vg/step = 0.1V, Offset = 1.8V, Rload=.10, N Steps = 10

6_1. Common drain amplifier component values

R_{G1}:		**R_{G2}:**		**R_S:**		**R_L:**		**Ri:**	
C_{in}:		**C_{out}:**		**C_{hi}:**		**C_{hi2}:**		**Riso**	

6_2. Common-drain amplifier. There are 4 printouts (Vin, Vout, Power spectrum, and ACsweep). Assume $I_D = I_S$, Fgen = 5kHz. Rin = Vin / Iin, Rout = (Voc – Vout) / I_{load}

DC Q-Point:	V_{GS}:		V_{DS}:		I_D:	
	V_S:		V_G:		V_D:	
Gain:	Voltage:		Current:		Power:	
Voltage Output:	Max:		THD%:			
	Vin:		V_{Ri}		Iin:	
	Vload:		I_{LOAD}		Voc:	
Impedance:	Input		Output			
Frequency Response:	Low:		High:		BW	

6_3. Common-drain amplifier with a variable load resistor. There are no printouts here.

100Ω Resistor:

Gain:	Voltage:		Current:		Power:	
Voltage Output:	Max:					

27kΩ Resistor:

Gain:	Voltage:		Current:		Power:	
Voltage Output:	Max:					