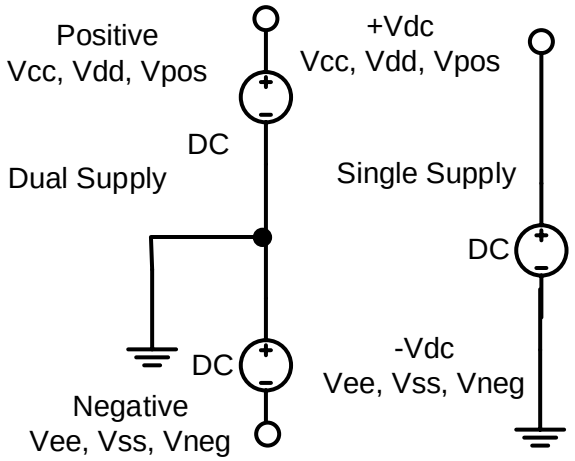
ECE 3274
Two-Stage Amplifier Project

1. Objective

The objective of this lab is to design and build a direct-coupled two-stage amplifier, including a common-source gain stage and a common-collector buffer stage. We will be online this semester and need to build the circuit at home we will use power supplies Vpos = 12Vdc Vneg = 0Vdc. We will use a single supply in the lab classroom if in person this semester.



2. Components

Qty	Device
1	2N3904 BJT Transistor
1	2N7000 MOSFET Transistor

3. Introduction

Multistage amplifiers made up of single transistor amplifiers connected in cascade. The first stage usually provides a high input impedance to minimize loading the source (transducer). The middle stages usually account for most of the desired voltage gain. The final stage provides a low output impedance to prevent loss of signal (gain), and to be able to handle the amount of current required by the load.

When analyzing multistage amplifiers, the loading effect of each stage must be considered, since the input impedance of the next stage acts as the load impedance for the previous stage. Therefore, the ac analysis of a multistage amplifier is usually done starting with the final stage. The individual stages are usually coupled either with a capacitor, or by direct coupling. Capacitive coupling is most often used when the signals being amplified are ac signals. With capacitive coupling, the stages are separated by a capacitor, which blocks the dc voltages between each stage. This dc blocking prevents the bias point of each stage from being upset. DC coupling requires more attention to detail in the bias network, but allow for good low-frequency response (usually down to dc).

The CS-CC cascade two-stage amplifier is a good multistage configuration because the CS and CC amplifiers together provide some very desirable characteristics. The CS amplifier makes up the first stage and is capable of providing high voltage gain. The input impedance of the CS is a function of Rg1 and Rg2 and is generally very high. The output impedance of the CS is approximately equal to $R_d \parallel r_0$, which is usually in the kΩ range. The CC amplifier makes up

the second stage and has the characteristics of high input impedance, very low output impedance, and high current gain.

In a cascade configuration, the overall voltage and current gains are given by:

A_V overall = A_V input stage * A_V Output stage

Note: The AV of Input stage includes the input voltage divider.
The Av of the output stage includes the output voltage divider.

A_I overall = A_I first stage * A_I second stage

In designing this amplifier, it is highly recommended that you take advantage of the work you did in the Common-Collector and CS MOSFET amplifier labs. You may need to make modifications to your work, but on the whole these amplifiers should be very good starting places. You need not show your work on the bias points, but you should show how you calculate all *overall* values in this lab.

You should refer to your lab lecture notes, your Electronics II Lecture notes, your textbook, the course website, and other reference material to determine how best to design your amplifier. This lab is intended as a design project and not as a step-by-step guide.

4. Requirements

Your amplifier design must meet the following requirements.

Requirement	Specification
Voltage Gain of Amplifier	Open loop, Rsf = 0
F_L Low Frequency Cutoff	Between 100 Hz and 300 Hz
F_H High Frequency Cutoff	Between 40 kHz and 150 kHz (set to 100kHz)
Overall Input Impedance (Rin)	Between 5KΩ and 10KΩ
Choose Output Voltage	Between $2V_{pk\text{-}pk}$
Load Resistance (CC) Rload	220Ω
Vrs Voltage across Rs	2.0Vdc
Vre Voltage across Re	6Vdc
Power Supply Voltage	Single Vpos= +12Vdc Vneg = 0Vdc

Table 1. Two-stage amplifier requirements.

5. Prelab Design Project

You will design the two-stage in this prelab design project. You should start with your previous designs for a common-collector and common-source amplifier as reference to work from, and modify them (if necessary) to meet the requirements for this lab. Then calculate values for the new components. Remember the input impedance of the CC is the load impedance of the CS.
The voltage on drain (Vd) is the bias voltage on the base (Vb).
You must be included, the schematics, show all calculations with the equations, and any assumptions you made. Units must be included as well as is recommended real component values. **Amplifier gain is open loop so Rsf = 0**

Use these values for the transistors: BJT, and MOSFET
For the BJT 2N3904 Use **roCC = 18 KΩ**, **β = 165, VceSat = 0.2Vdc**
For the MOSFET 2N7000 use V_{GS} = 2.1Vdc, Use **roCS = 8kΩ from your CS amp lab, VdsSat = 1.0Vdc** and **gm = 0.007**

Note: You may find that the High frequency breakpoint will be lower than your design values be of the internal capacitance of the MOSFET. The AVcs will CS stage is control gain using Rsf and Rsb. The gain Av will be higher in both LTspice and the built circuit, adjust the input voltage Vin get the required output voltage Vout. Make your measurements at that setting. The AvCS must compensate for gains of less than one of the AvCC , Input voltage divider, and Output voltage divider.

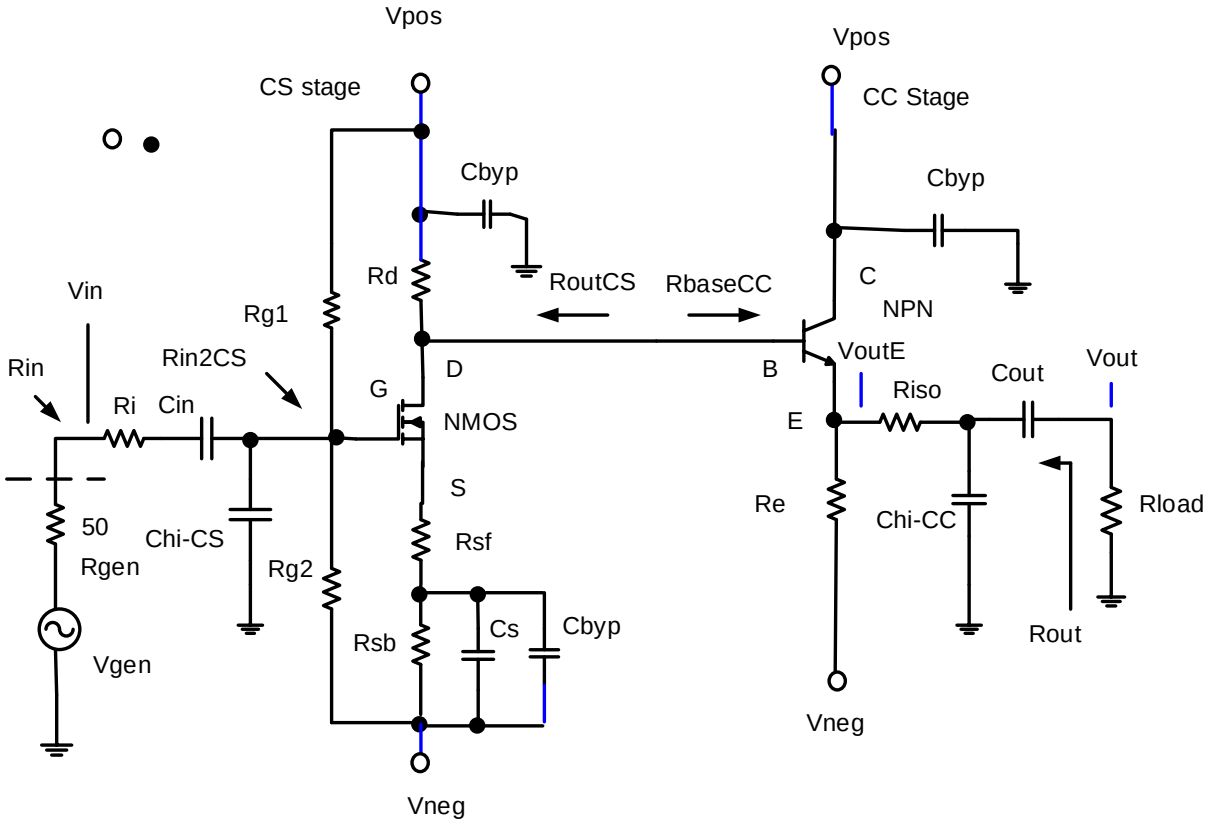


Figure 1. Two-stage amplifier circuit.

Component	Value
R_i	150Ω
Riso	47Ω
C_{byp}	0.1µF, 0.047uF, or 0.01uF

Table 2. Fixed component values.

5.1. DC Bias

Begin by designing the DC bias for the CC amplifier stage based on output requirements. Note that the location and value of the capacitors do not affect the DC biasing. Once you have designed the DC bias, use the transistor characteristics for the 2N3904 and 2N7000 transistors to determine the transistor parameters for where you are operating. Note that there is no single correct answer and that your design may differ significantly from your colleagues'. You must show all work and walk through all calculations.

Component Values	Amplifier Parameters	Voltages and Currents
R_{G1}, R_{G2}	Beta ac and dc (2N2904)	V_{ce}, V_{be}, V_e
R_D, R_S	r_π, r_o, β (2N3904)	I_b, I_c
	V_{TN}, r_o, g_m (2N7000)	V_{GS}, V_{DS}, V_S
R_e		I_D

Table 3. DC Bias and Amplifier Parameters

5.2. AC Analysis

Once you have designed the bias network and determined the transistor parameters, you are ready to begin the ac analysis. Table 4 shows all of the values you need to calculate. Be sure to show all work. You may use equations given in the lab lecture, class lecture, or from a textbook (i.e., you do not need to derive the voltage gain). Be sure you understand how to use the equations, though—if assumptions are included, you must state these and show that you meet them. Do not simply copy equations out of the book and use them, because they probably won't work.

Use the Short-Circuit Time Constant method to determine the capacitor value

$BWshrinkage = \sqrt{2^{1/n} - 1}$ Where (n) number poles or zeros at the same frequency.

Determine the capacitor value for **CinCS**, **Cs** and **CoutCC** by setting each time constant to a frequency of **F_L* BWshinkage with n = 3**. Determine the capacitor value for **Chi-CS**, and **Chi-CC** by setting each time constant to a frequency of **F_H / BWshinkage with n = 2.**

Component Values	Amplifier Parameters	Voltages, Currents, and Power
C_{in}	Overall Voltage Gain	v_{in}
C_{out}	Overall Current Gain	v_{out}
C_s	Overall Power Gain (in dB)	i_{in}
	Overall Low Frequency Cutoff	i_{out}
Chi-CS	Overall High Frequency Cutoff	p_{in}
Chi-CC	Overall Input Resistance	p_{out}
	Overall Output Resistance	

Table 4. Small Signal (ac) Amplifier Parameters

5.3. Computer-aided Analysis (25 Points)

Once you have completed your amplifier design, use LTspice to analyze their performance. Generate the following plots for each amplifier design: include LTspice schematics.

(a) A time-domain plot of the input and output, with the output voltage of $3V_{pk\text{-}pk}$ or greater at 5 kHz. The output should not have any distortion or clipping. Calculate the midband gain and indicate it on the plot. Compare this to your calculated values.

(b) An FFT of your time-domain waveform. Circle and indicate the height of any strong harmonics, in dB relative to your fundamental frequency at 5 kHz.

(c) A frequency sweep of the amplifier from 10 Hz to 1 MHz. Indicate the high and low frequencies on the plot (these should correspond to the half-power, or -3dB points). Compare these to your calculated values.

5.4. Prelab Questions

(a) What would happen if you swapped the order of the transistors?

(b) Could you use a CE amplifier in place of a CS amplifier, and/or a CD amplifier in place of a CC amplifier? Why or why not? What restrictions.

(c) What would be the advantages and disadvantages of replacing the CC output stage amplifier with a push-pull amplifier stage?

6. Lab Procedure

6.1. Construct the amplifier shown in Figure 1. Remember that R_{GEN} is internal to the function generator and the shunt Ri = 150. Also remember to use two emitter resistors of approximately the same value, as shown in the schematic. Record the values of the bias network resistors and the capacitors you used in the circuit.

6.2. Measure the following values:

(a) Q-point: Vce, Vbe, V_E, V_C, V_B, and Ic (2N3904), and V_{DS}, V_{GS}, V_S, V_D, V_G, and I_D (2N7000).

(b) Voltage gain each stage

(c) Overal**l** voltage, current, and power gains.

(d) Maximum undistorted peak-to-peak output voltage (Vout).

(e) Overall Input and output resistance. At 5kHz

(f) Low and high cutoff frequencies (half power point).

Recall that input impedance is given by $R_{in} = v_{in}/i_{in}$, output impedance is given by $R_{out} = (v_{oc}-v_{load})/i_{out}$, voltage gain is given by $A_v = v_{out}/v_{in}$, and current gain is given by $A_i = i_{out}/i_{in}$.

Additionally, plot the following:

(a) Input and output waveform at the maximum undistorted value.

(b) FFT showing the fundamental and first few harmonics.

(c) Frequency response from 10 Hz to 1 MHz (set the input voltage to a value that does not cause distortion across the entire passband of the amplifier).

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Data Sheet

Name: _____ **Lab Date:** _____ **Bench:** _____

Group: _____ **CRN:** _____

Remember to include units for all answers and to label all printouts. There are a total of three (3) printouts in this lab. Up load Report data sheet, plots, and **photo** of as built circuit.

6.1. Component Values

R_{G1}:		**R_{G2}:**		**R_{Sf}:**		**R_{sb}:**	
Rd:		**Re:**		**R_{iso}:**	47	**Ri:**	150

6.2. Two-stage amplifier. There are three printouts here.

Capacitor Values:	C_{in}:		C_{out}:		C_{hi}CS:	
	C_s:				C_{hi}CC:	
Q-Point: DC values	V_{ce}:		V_{be}:		I_C:	
	V_E:		V_B:		V_C:	
	$V_{GS:}$		V_{DS}:		I_D:	
	V_S:		V_G:		V_D:	
Gain include divider	Av CS		Av CC			
Overall Gain:	Voltage:		Current:		Power:	
Voltage Output Vpp:	Max:					
Resistance: at 5kHz	Input		Output			
Frequency Response:	Low:		High:		BW:	

Include plots: Maximum output voltage at 5kHz, Frequency Response plot.