Experiment: The Flyback DC-DC Converter

Objective

The objective of this experiment is to understand the operating principles of the Flyback DC-DC converter and evaluate its performance under different simulation scenarios using LTSPICE and actual circuit building.

References

[1] R. W. Erickson, D. Maksimovic, "Fundamental of Power Electronics," 2nd Edition, Kluwer Academic Publishers, 2004.

[2] R. Ridley, "Flyback Converter Snubber Design", Available [Online]: http://www.ridleyengineering.com/images/phocadownload/12_%20flyback_snubber_design.pdf

Introduction

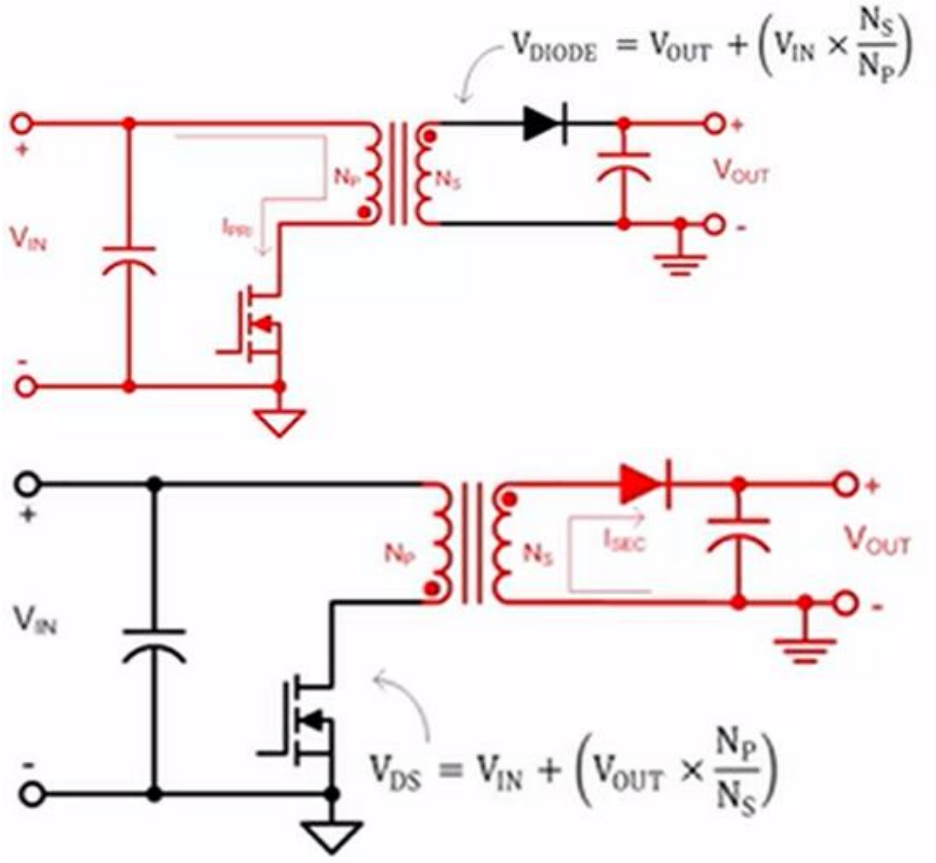
The Flyback converter is an isolated DC-DC converter that uses mutually coupled inductor (transformer) to store energy. When the current passes through the primary and release the energy to the secondary when the power is removed. The Flyback converter and the Buck-Boost converter are similar in operation and performance. However, in the Flyback converter, the primary and secondary windings are used as two separate inductors. The advantages of the Flyback topology include isolation between the primary and secondary sides of the converter, the ability to support multiple outputs, the ability to operate with a wide range of input voltages, higher voltage gain and low parts count. This converter is used in low- to mid-power applications where the power rating is around several hundred Watts.

The basic topology of the Flyback converter is shown in Fig. 1. The topology consists of an input capacitor C_{in}, a primary-side switch Q, usually a MOSFET, a coupled inductor called the Flyback transformer T, an output rectifier D_{out} and an output capacitor C_{out}. Careful design of the turns ratio between the primary and secondary side enables the output voltage to be higher or lower than the input voltage. In addition, isolation is provided by the Flyback transformer. By adding more windings to the transformer, multiple outputs can be supported. The Flyback transformer oversees energy storage, energy transfer and isolation. Hence, the need for an output low-pass filter is eliminated.

(a) (b)

Fig. 1. (a) The basic topology of the Flyback Converter and (b) The Flyback converter with multiple outputs.

All Flyback converters have the same operating principle. As shown in Fig. 2 (a), energy stored in the transformer when the MOSFET switch Q is turned on. Because of the reverse dot signs of the transformer, the diode on the output side will be reverse biased. This mode is called the ON time of the converter. During ON time, input voltage is applied to the primary side of the transformer and the output is supplied by the output capacitor. The input current rises linearly in proportion to the input voltage. The MOSFET switch Q is turned off when enough energy is stored in the transformer. The diode can now conduct and deliver the energy to the load. This operating mode is shown in Fig. 2 (b). It should be noted that the diode and the MOSFET Q should never conduct at the same time. This mode is called the OFF time of the converter. During the OFF time, the current continues on the secondary side of the transformer. The current decreases linearly in proportion to the output voltage. The primary side is now an open circuit.



(a) (b)

Fig. 2. Equivalent circuit of the Flyback converter (a) during ON time and (b) during OFF time.

There are several operating modes for the Flyback converter. Examples include continuous conduction mode (CCM), discontinuous conduction mode (DCM), quasi-resonant mode (QR), boundary mode etc. In this experiment, only CCM will be studied. In CCM, a continuous current is flow through the transformer during each switching cycle. When Q is turned ON, the primary current ramps up. However, it does not start from zero Amps. This is because of the residual energy that is continuously maintained in the transformer. When Q is off, the transformer demagnetizes resulting in the secondary current ramping down. However, it does not decrease all the way to zero Amps. This is because the next switching cycle begins before the current is completely depleted. The advantages of CCM are small ripple and rms currents, lower capacitor loss, lower MOSFET conduction and turn-off loss, lower core losses and smaller EMI and output filters. DCM operation is achieved by designing the power stage such that the transformer is allowed to completely demagnetize during each switching cycle. During ON time, the primary current ramps up from zero Amps. During the OFF time, the secondary current ramps down to zero Amps. The time instance when both primary and secondary currents are zero is called dead time. The advantages of operating the Flyback converter in DCM include no diode reverse recovery losses and lower inductance value. In boundary operating mode, the secondary current reaches zero when the primary current starts from zero.

Steady-State Analysis of the Flyback Converter in CCM

To analyze the Flyback converter in steady state, the transformer in Fig. 1 (a) needs to be replaced with its equivalent model, including its magnetizing inductance. This model is shown in Fig. 3. We can now begin analyzing the circuit during ON time and OFF time. During ON time, the primary side is connected to the input, the diode is reverse-biased, and the output is supplied by the capacitor. The equivalent circuit for this mode is shown in Fig. 4 (a). During this mode, the inductor voltage v_L, capacitor current i_C, and DC source current i_g are given by

$$v_L = V_g$$
$$i_c = -\frac{V}{R}$$
$$i_g = i$$

By assuming that the inductor current ripple and capacitor voltage ripples are small, the magnetizing current and output capacitor voltage can be substituted by their DC components, I and V, respectively. Therefore,

$$v_L = V_g$$
$$i_c = -\frac{V}{R}$$
$$i_g = I$$

During OFF time, the primary side is open, the diode conducts, and the load is supplied by the secondary side. The equivalent circuit for this mode is shown in Fig. 4 (b). The equations now become

$$v_L = -\frac{V}{n}$$
$$i_c = \frac{I}{n} - \frac{V}{R}$$
$$i_g = 0$$

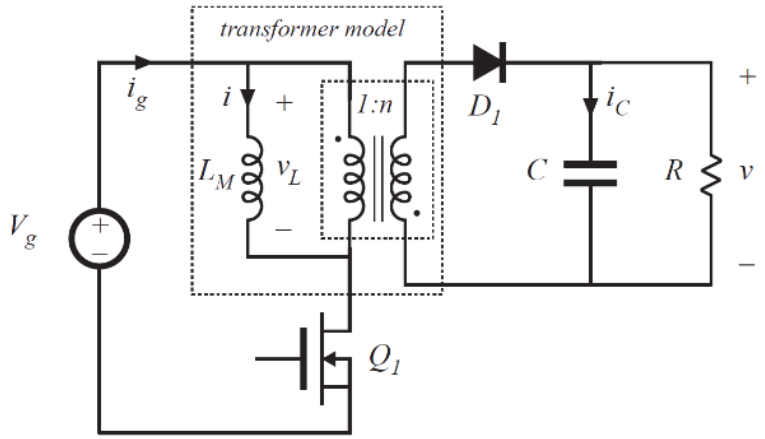
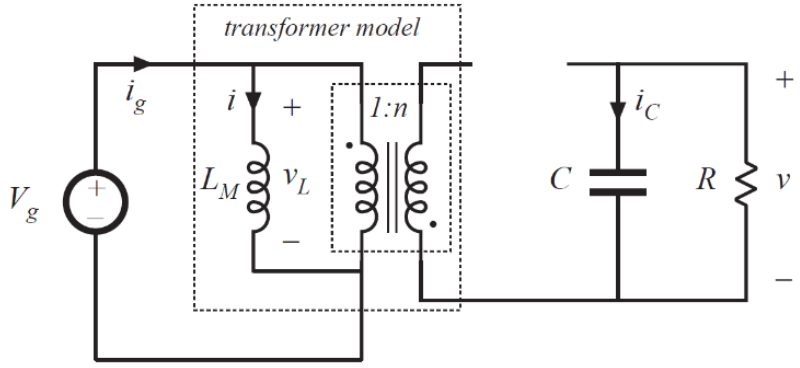
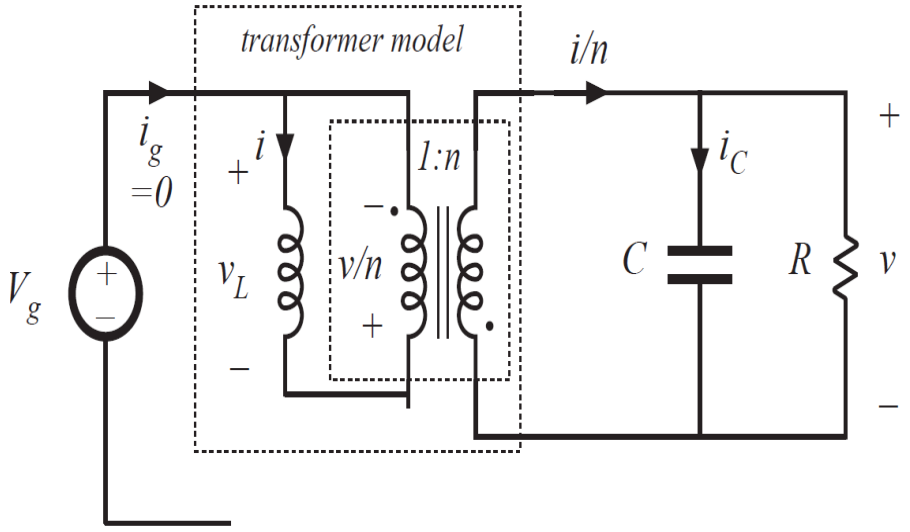


Fig. 3. The Flyback topology including detailed transformer model.



(a)



(b)

Fig. 4. Equivalent circuit of the Flyback converter during (a) ON time and (b) OFF time.

Steady state values for CCM mode:

The waveforms for the mentioned variables in CCM are shown in Fig. 5. Due to Volt-Second balance, the average value of v_L is zero. Hence, the conversion ratio between the average output voltage and average input voltage is found as

$$M(D) = \frac{V}{V_g} = n\frac{D}{D'}$$

where $D' = 1 - D$.

The average capacitor current is also zero due to Capacitor Charge balance. Hence, the average value of the magnetizing current is found as

$$I = \frac{nV}{D'R}$$

The average value of the input current is found as

$$I_g = DI$$

Hence, the conversion ratio between the output current and the input current is found to be

$$\frac{I_g}{I_o} = \frac{nD}{D'}$$

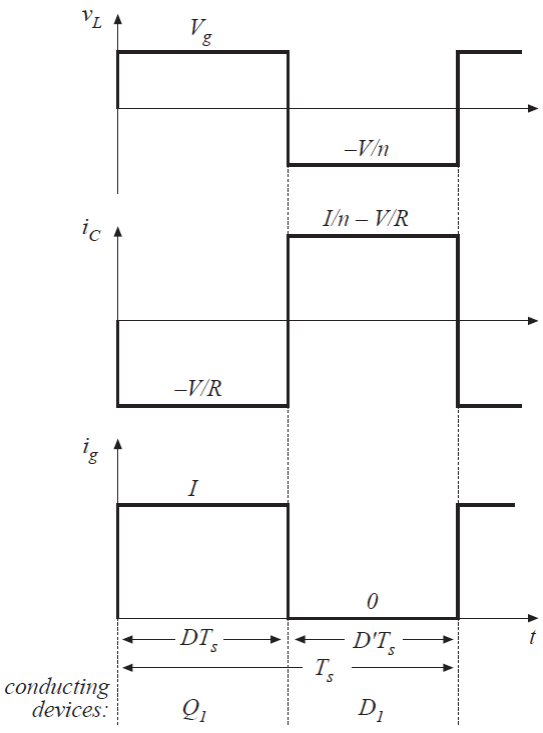


Fig. 5. The Flyback converter waveforms for CCM.

Steady state values for DCM mode:

However, for DCM mode of operation, The relationship between Input and output voltage is given by the following equation.

$$\frac{V_o}{V_{in}} = \frac{D}{\sqrt{K}}$$

Here “K” relates to circuit parameters as:

$$K = \frac{2 \, . \, L_s}{R \, . \, T_s}$$

Where,

L_s is the Secondary Inductance

R is the Load resistance

T_s is the switching time period

Snubber Circuit Design

All PWM converters have non-ideal parasitic that lead to ringing waveforms to be suppressed. Otherwise, switches will be prone to failure and noise levels will be undesirable. In the Flyback converter, the turn-off of the power switch interrupts current through the leakage inductance of the transformer which will cause a voltage spike on the drain of the MOSFET. The inductance will then ring with stray capacitances in the circuit, producing large amplitude high-frequency waveforms. The ringing waveforms will cause excessive voltage on the MOSFET which might lead to an avalanche breakdown and failure of the device. The ringing waveforms will also cause noise issues and logic errors. In most designs, this is not acceptable. Therefore, circuit elements are required to be added to damp the ringing or clamp the voltage or both. These circuits are called snubber circuits. In this procedure, design of a primary RC snubber circuit will be explored.

A Flyback converter with a primary RC snubber circuit is shown in Fig. 7. The resistor provides damping for the LC resonance of the power circuit and the series capacitor prevents the voltages at the power stage switching frequency from being applied across the resistor.

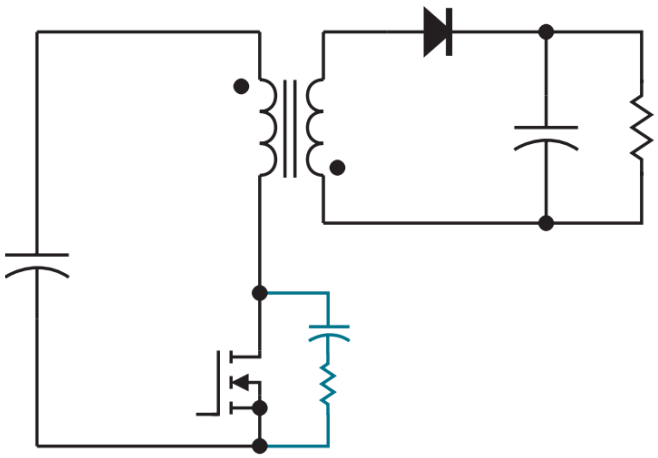


Fig. 7. Flyback topology with primary RC snubber.

Suggested Procedure :

LTSPICE simulation

Build the circuit shown in Fig. 8 in LTSPICE environment. The supply voltage is 5V. The switching frequency is 50kHz. Assume that the efficiency of the circuit is 100%.

Run the simulation with no series resistance added to both primary and secondary windings of the transformer T1. Observe the steady state (after running the simulation for around 300 ms) output voltage, output current, primary current and secondary current by varying the duty cycle from 10% to 80% and fill out Table.1. Also, provide the respective plots containing traces for various duty cycles (4 plots in this part with each plot containing 8 traces). What is the mode of operation for various duty cycles? Is it CCM or DCM? Confirm your results with the presented theory. As an example, you need to provide the detailed calculation of theoretical values of output voltages at 20% and 80% duty cycle in your report.

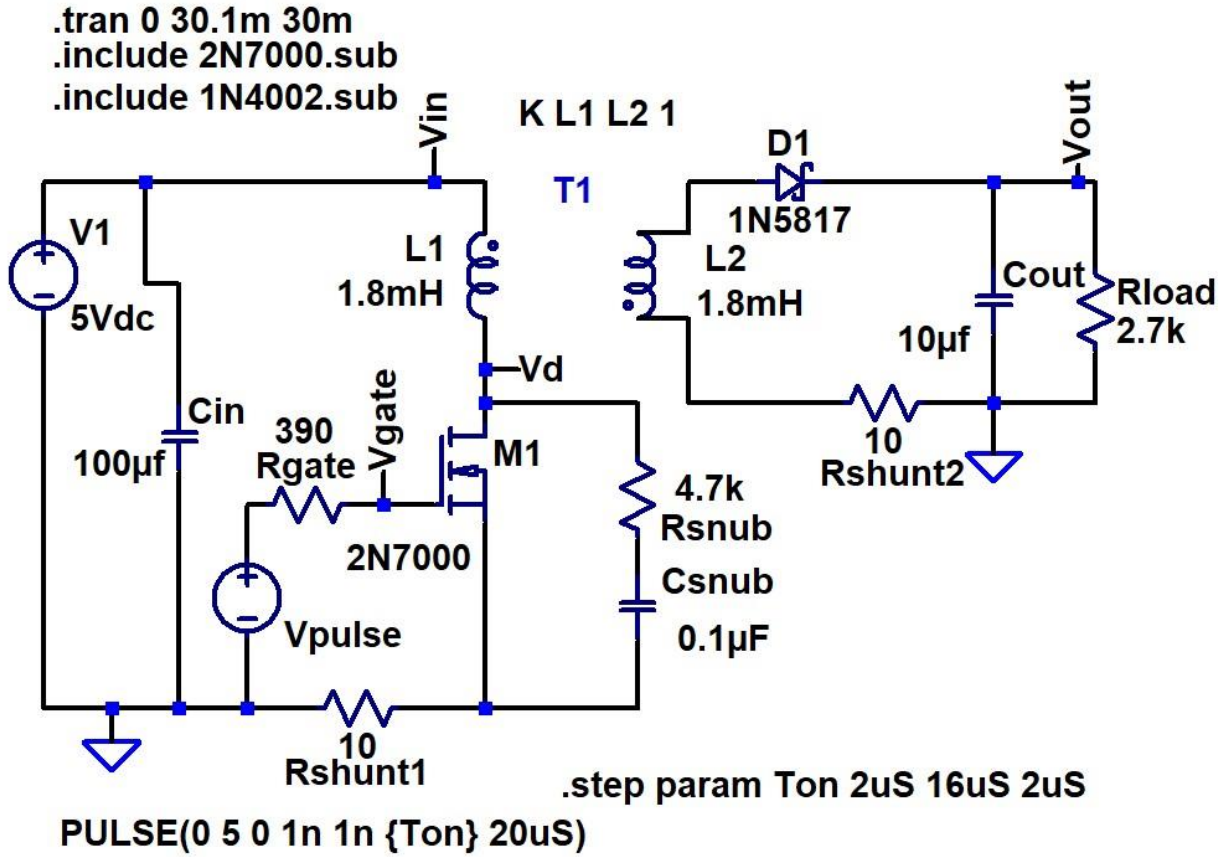


Fig. 8. Flyback topology for simulation in LTSPICE.

Table. 1. Output voltage and current, primary current, and secondary current vs duty cycle.

Note: Calculate the current by a voltage across a known resistance. The shunt resistance is 10Ω

Duty Cycle	Output Voltage		Output Current		Measured Transformer Currents	
	Measured	Calculated	Measured	Calculated	Primary (Rshunt1)	Secondary (Rshunt2)
10%						
20%						
30%						
40%						
50%						
60%						
70%						
80%						

Next, run the simulation with the value of **0.04 Ω of series** resistance and **parallel core resistance of 2KΩ** added to both primary and secondary windings of the transformer. Observe the steady state (after running the simulation for around 300 ms) output voltage, output current, primary current and secondary current by varying the duty cycle from 10% to 80% and fill out Table 2 also, provide the respective plots containing traces for various duty cycles (4 plots in this part with each plot containing 8 traces). What is the mode of operation for various duty cycles? Is it CCM or DCM? You will confirm these results with the experimental section results.

Table. 2. Output voltage and current vs duty cycle (including series resistance).

Duty Cycle	Measured Load parameters	
	Output Voltage	**Output Current**
10%		
20%		
30%		
40%		
50%		
60%		
70%		
80%		

Experimental Circuit verification:

Build the circuit shown in Fig. 9 on the breadboard using T1 as the student wound 1:1 transformer. Pay attention to the polarity of components.

The input DC voltage should be set to 5V and the current limit should be set to 200mA. Set the function generator to generate a pulse wave gate drive signal with an amplitude of 5V P-P and an offset of +2.5V (0V to 5V Pulse wave). The frequency of the Pulse wave should be 50kHz with a 10% to 80% duty cycle. The transformer is 1.8mH. You should use the blue cores and wind the inductor up to 16 turns. This will give you a 1.792mH inductor since the inductance ratio is $\boldsymbol{7\mu H/turns^2}$**. The transformer be wound with difference ratio and multiple secondary.** We will wind a 1:1 to keep the voltages low.

Before wiring check your transformer polarity.

Determine the transformer polarity

Mark your transformer polarity dot, apply a 1v peak to peak sinewave to one of the winding (primary) and positive signal input is the dot. Connect channel 1 of the scope to the primary where the signal source is connected. Connect channel 2 on the other winding (secondary) if the signal are in phase the positive scope lead is the dot indication of the secondary. If they are out of phase by 180 then reverse the secondary scope connection and check.

Rgate = 390Ω to provide isolation from function generator.

Rshunt1, Rshunt2 = 10Ω each. Measure or observe current waveform.

Ishunt = Vacross shunt / shunt resistance.

Rload = 2.7KΩ. Rsnub = 4,7kΩ. Csnub = 0.1uF. Cin = 100uF. Cout = 10uF.

The supply voltage is 5V.

The switching frequency is 50kHz pulse 0V to 5V

Change the duty cycle from 10%-80% and fill **Table 3**. Provide the following plots

1. Plot of primary current and secondary current at 20% duty cycle

2. Plot of primary current and secondary current at 80% duty cycle

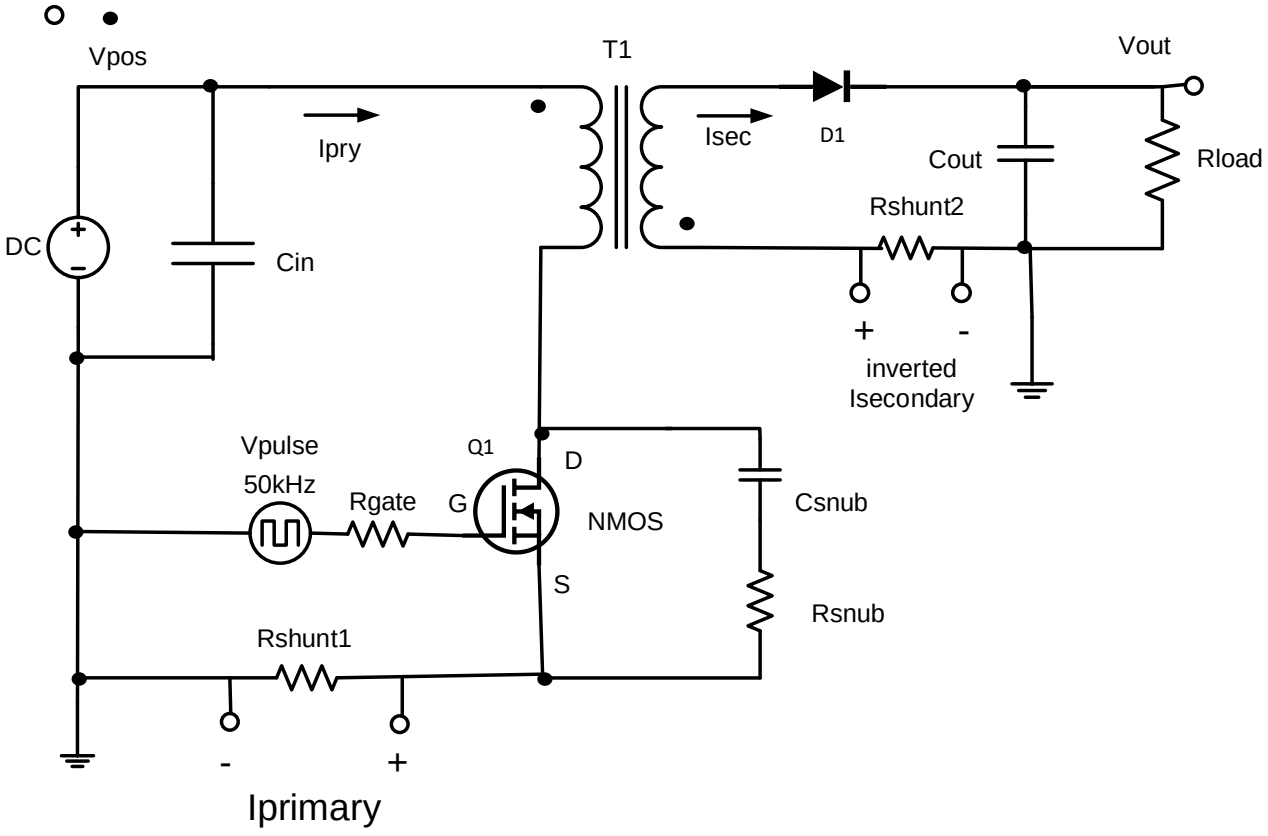


Fig. 9. Flyback topology for experimental circuit.

At a high duty cycle there is more time to charge the inductor so on the discharge cycle we do not fully discharge the inductor this is the Continuous Conduction Mode (CCM). Note as we decease the duty cycle, there is less charge time. The operating mode shifts to Discontinuous Conduction Mode (DCM) because now there the inductor will fully discharge.

Table. 3. Output voltage, primary and secondary currents vs duty cycle

Duty Cycle	Output Voltage Multimeter		Primary Current scope		Secondary Current Scope INV=on	
	Vo Oscilloscope	Mode CCM/DCM	Charge/discharge Ipp mA	Offset mAdc	Charge/discharge Ipp mA	Offset mAdc
10%						
20%						
30%						
40%						
50%						
60%						
70%						
80%						

Suggested Report Structure

Your hand-written report must include

1. Brief theoretical analysis of the functioning of the Flyback converter.

2. Simulation results including necessary plots of primary current, secondary current, and output voltage/current (8 plots) along with discussion and Tables. Provide the schematic in the report.

3. Experimental results (3 plots) including necessary plots along with discussion and Table. Provide a picture of the circuit build on the breadboard in the report.

4. Conclusions and evaluation of the Flyback converter's performance.